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Factoring integers with ECM on the Kalray MPPA-256 processor

Jérémie Detrey

CARAMBA team, LORIA

INRIA Nancy – Grand Est

Jeremie.Detrey@loria.fr

Joint work with:

Masahiro Ishii (NAIST, Nara, Japan)

Pierrick Gaudry (CARAMBA team, LORIA)

Atsuo Inomata (NAIST, Nara, Japan)

Kazutoshi Fujikawa (NAIST, Nara, Japan)

Context: Integer factorization

- Central problem in public-key cryptography:
  - integer factorization is a (supposedly) difficult problem
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- Current (publicly known) record:
  - factorization of the RSA-768 challenge (768 bits, or 232 digits)
  - the computation took $\sim$ 2000 core-years [Kleinjung *et al.*, 2010]

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Outline of the talk

- ECM in a nutshell
- The Kalray MPPA-256 processor
- Multiprecision modular arithmetic
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  - if K is finite, then so is $E(K)$

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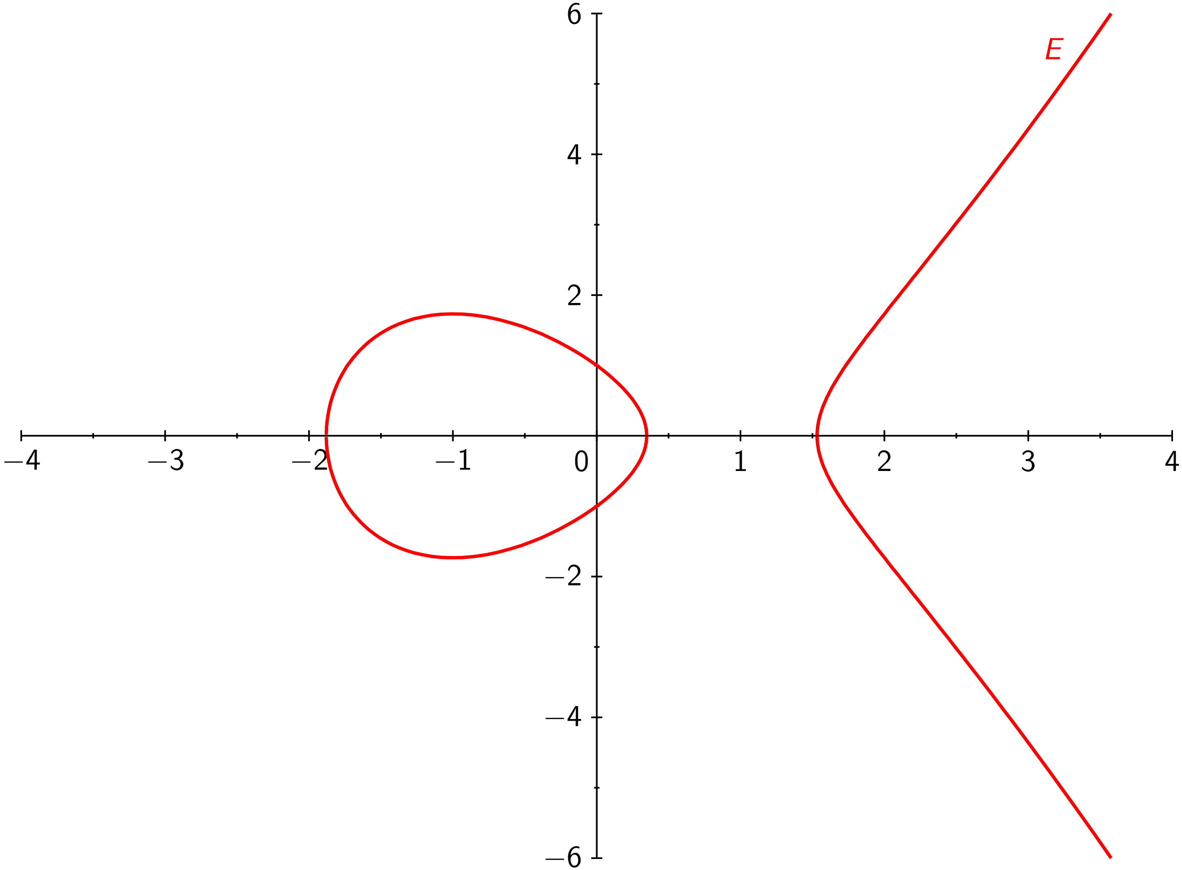

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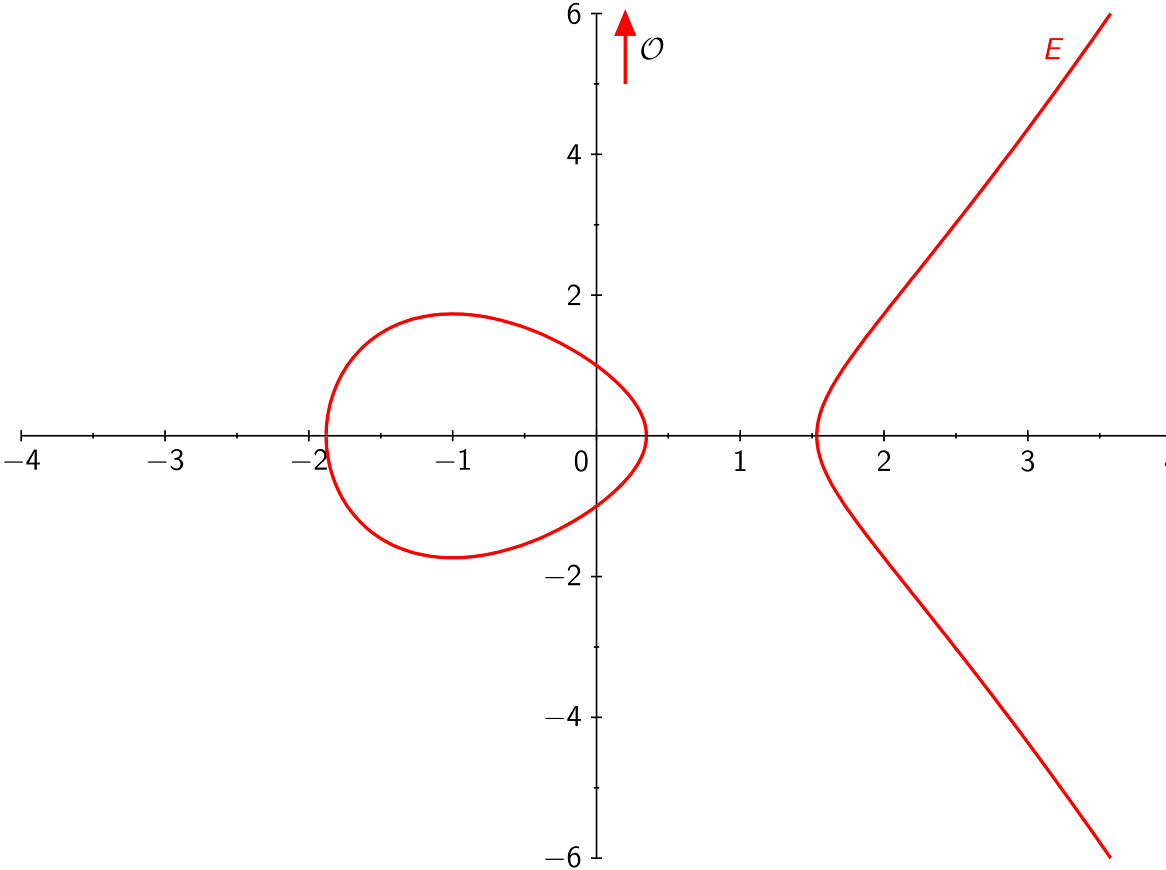

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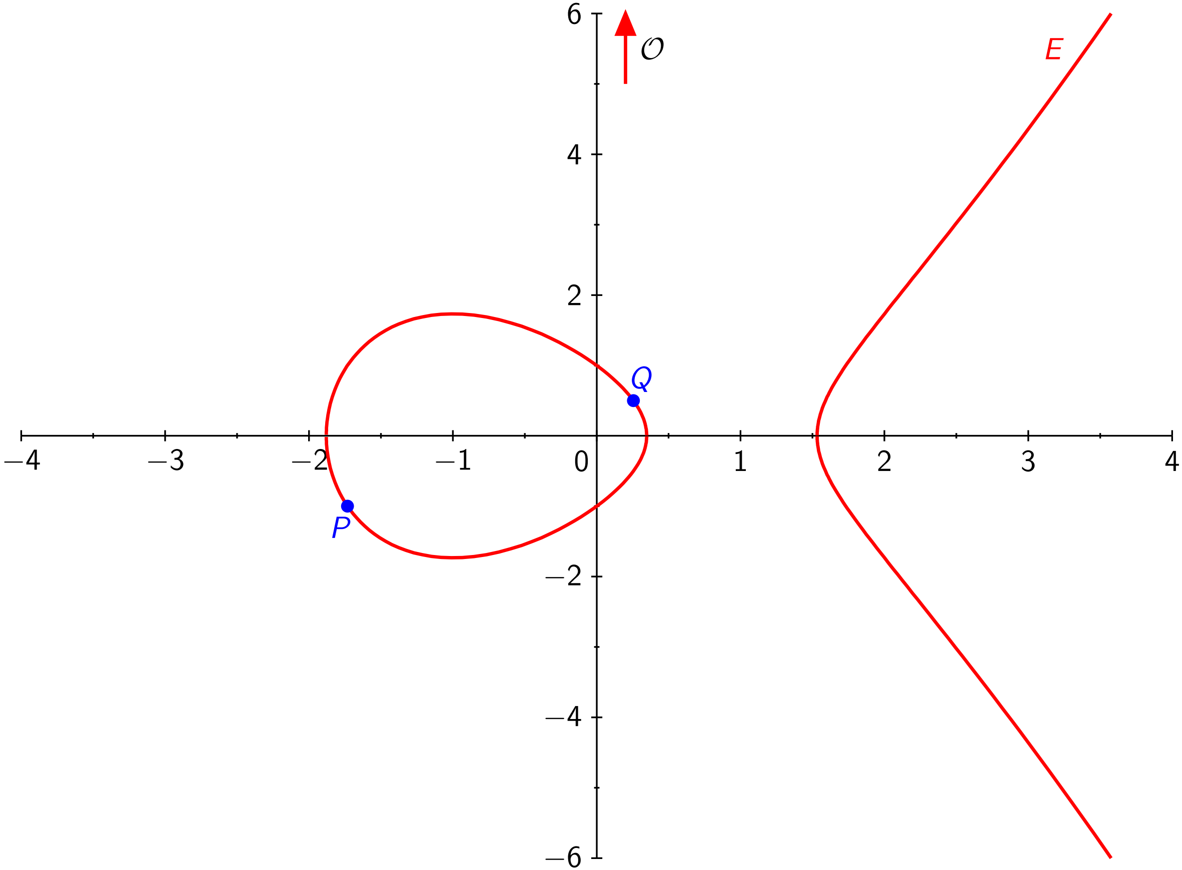

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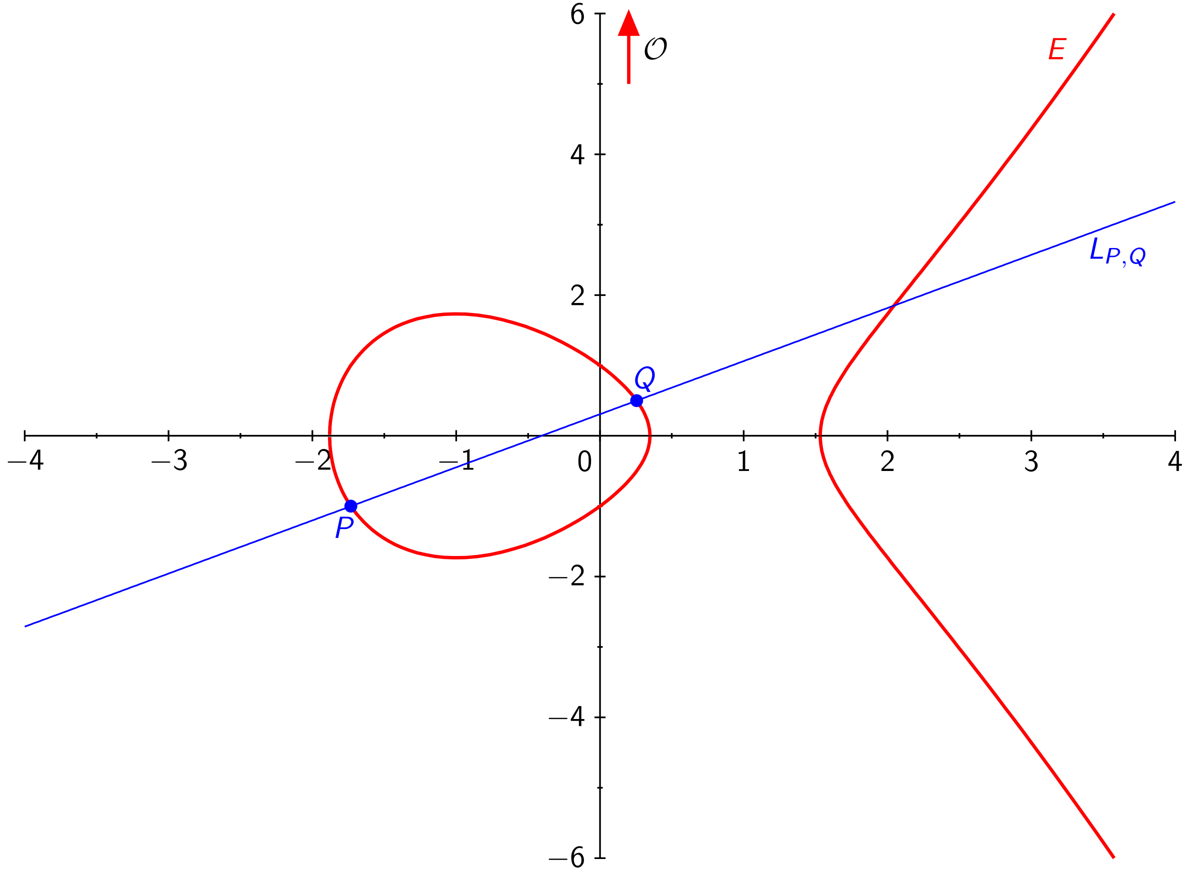

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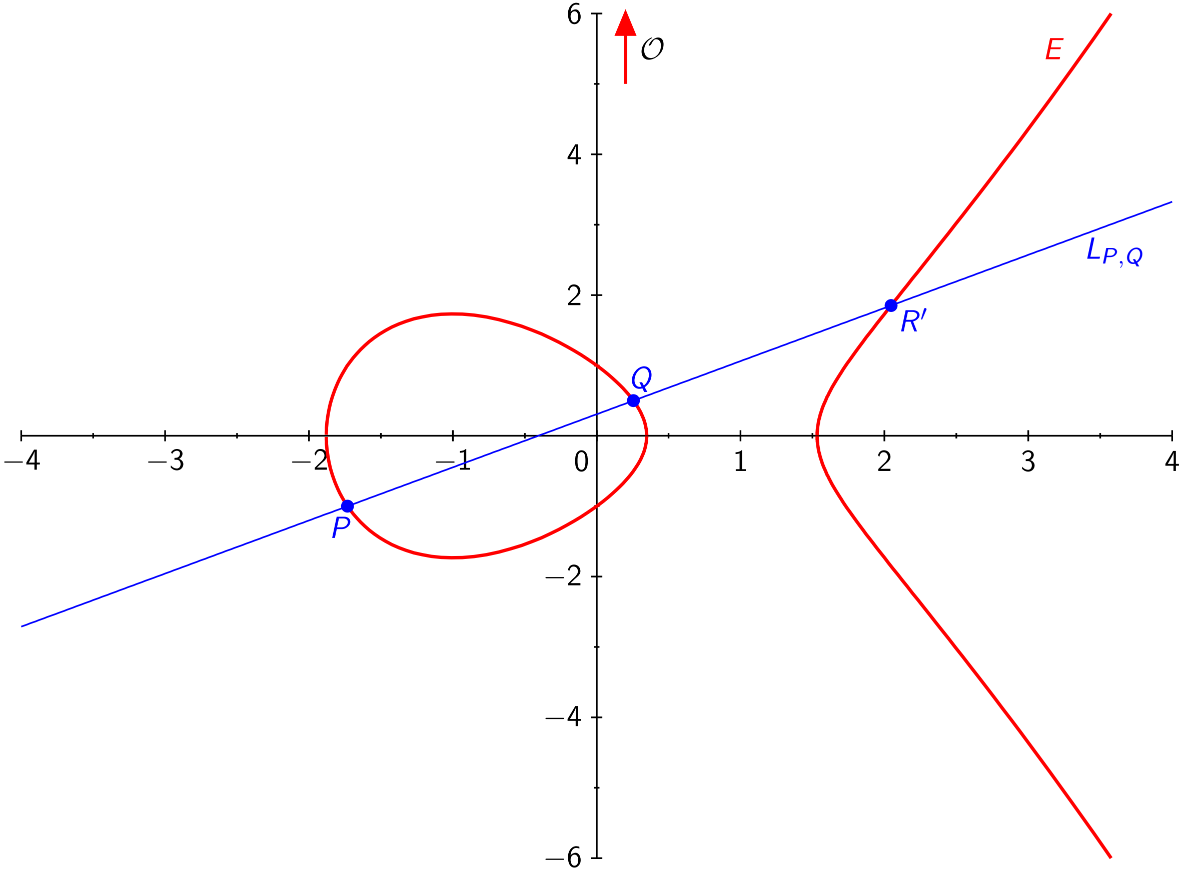

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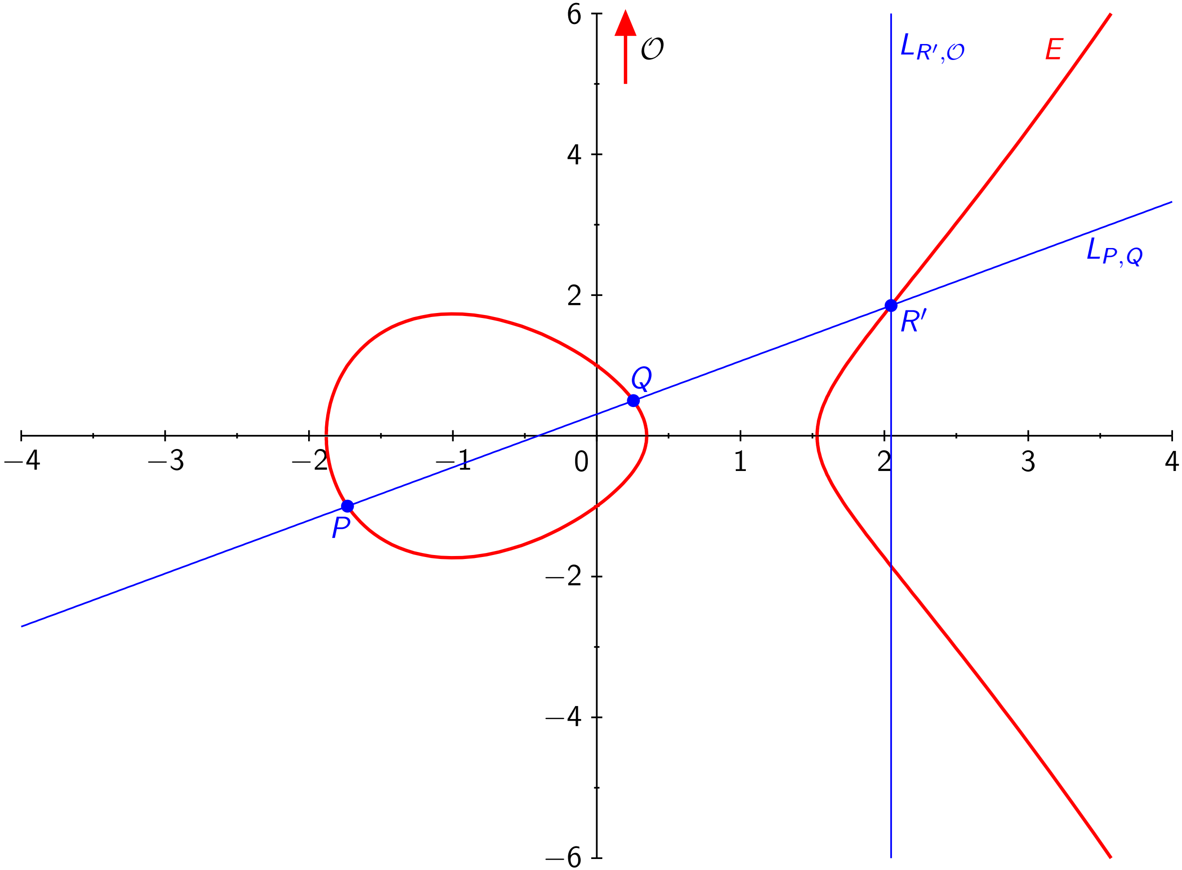

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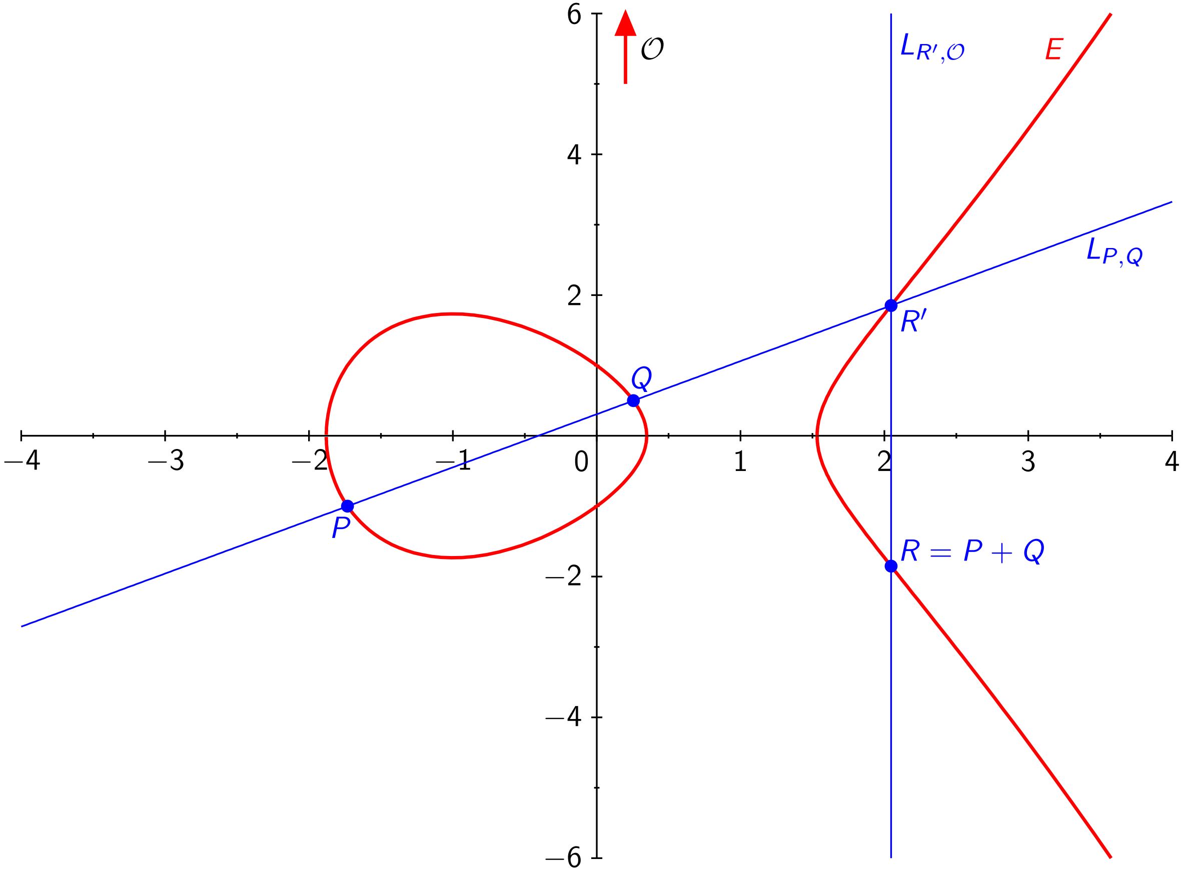

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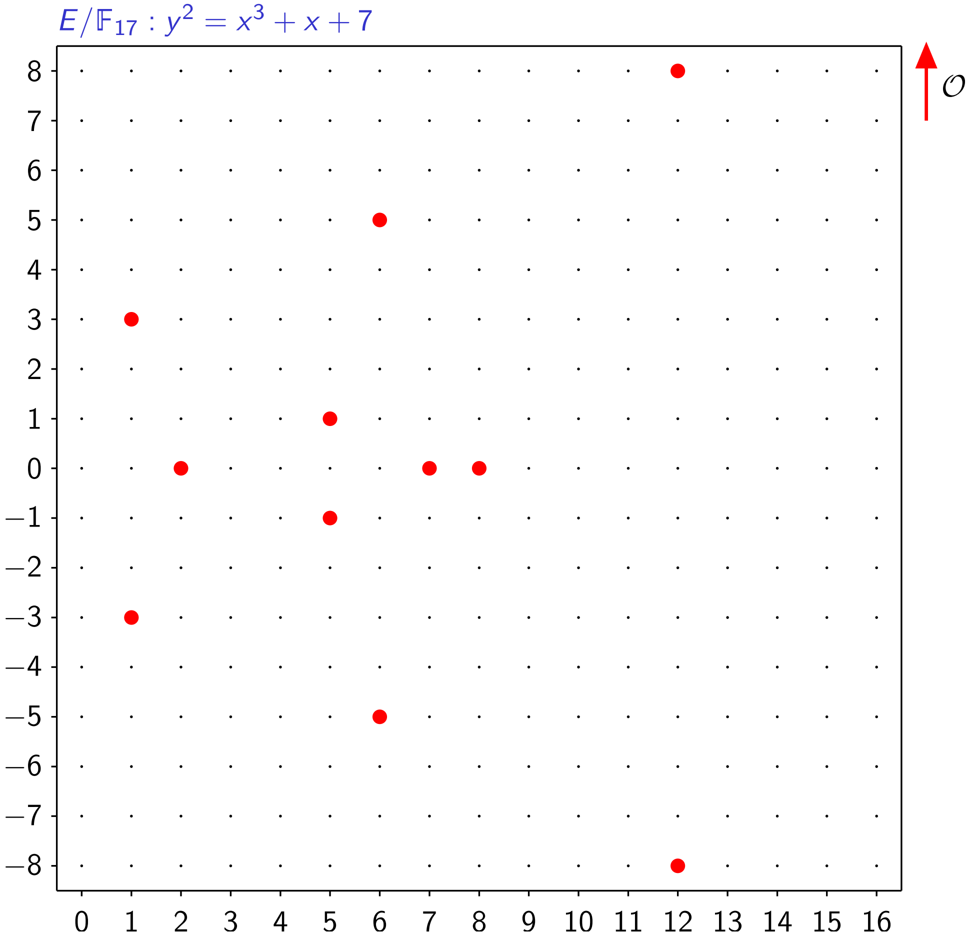

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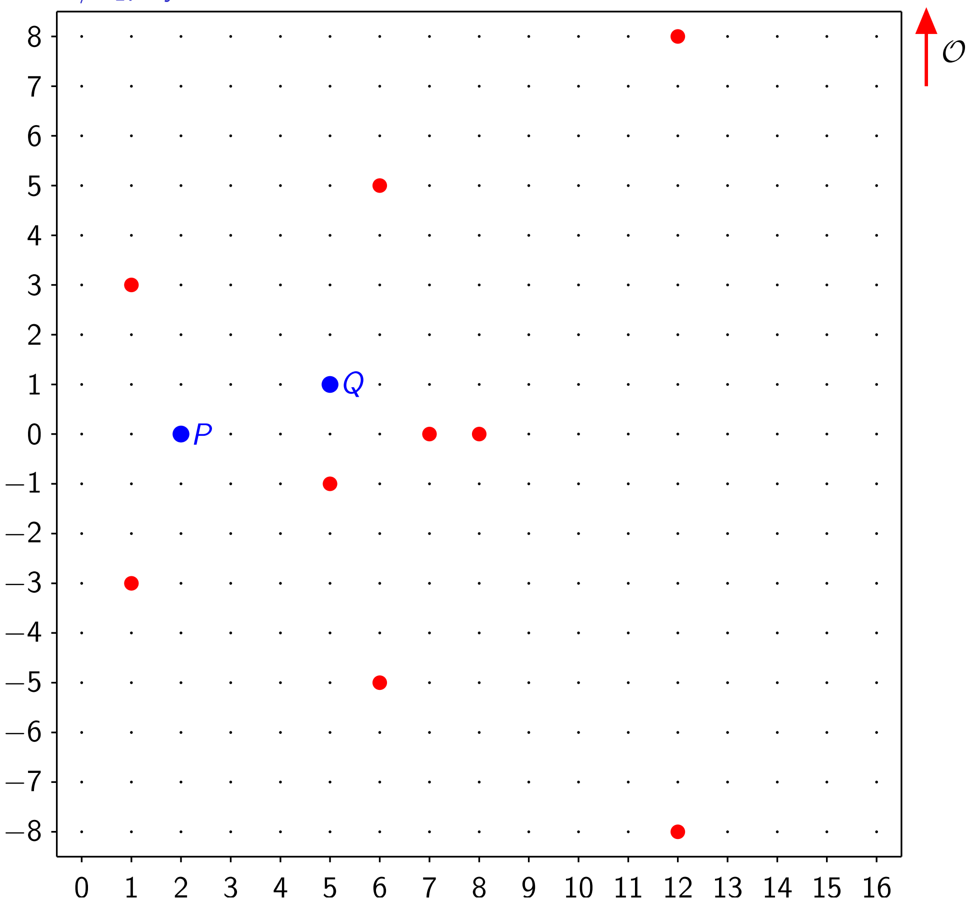

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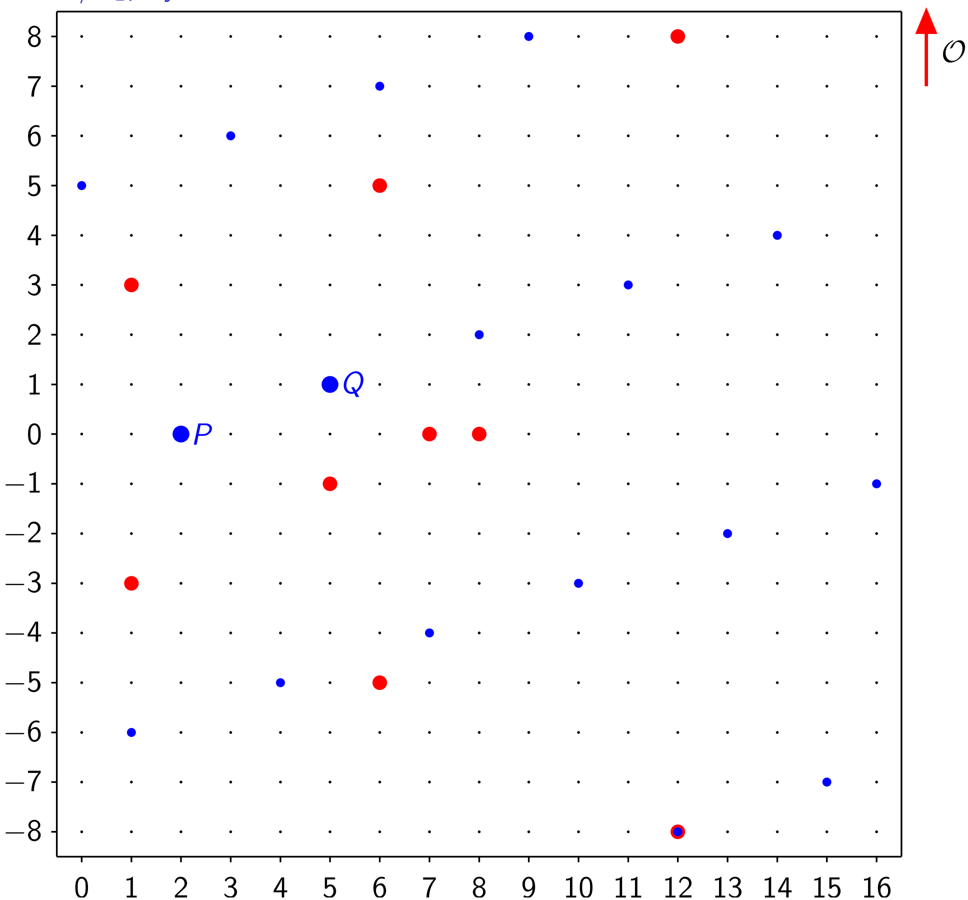

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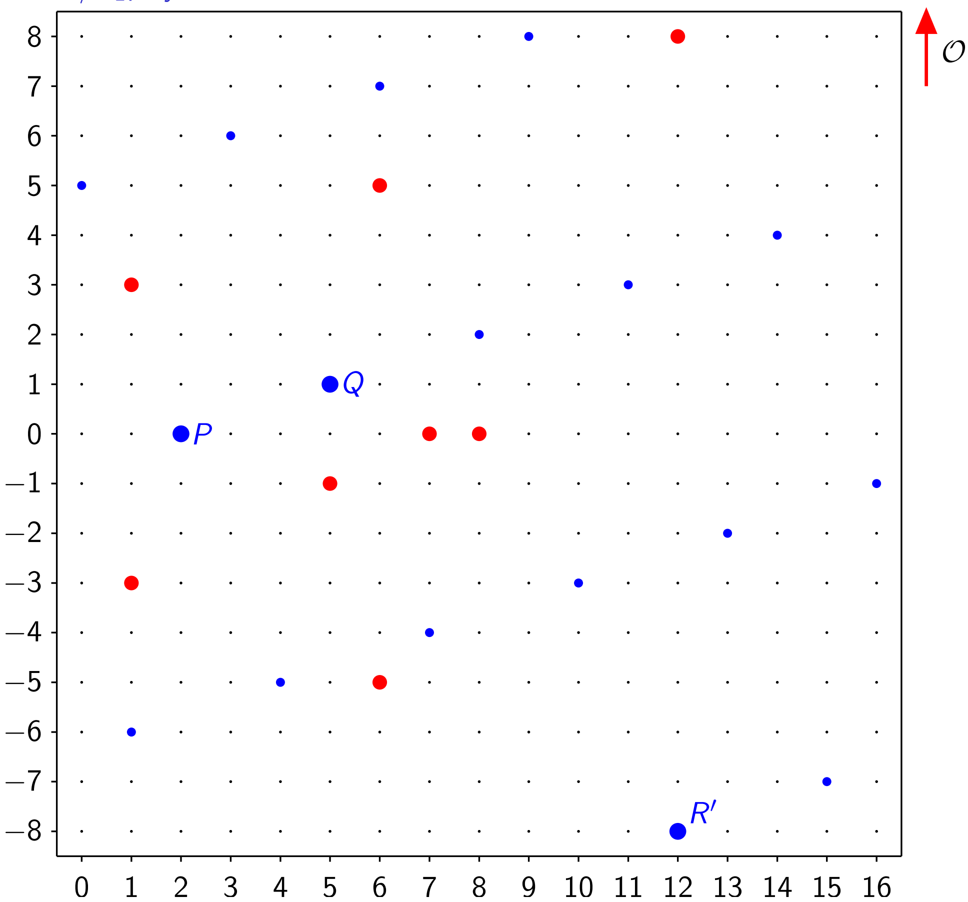

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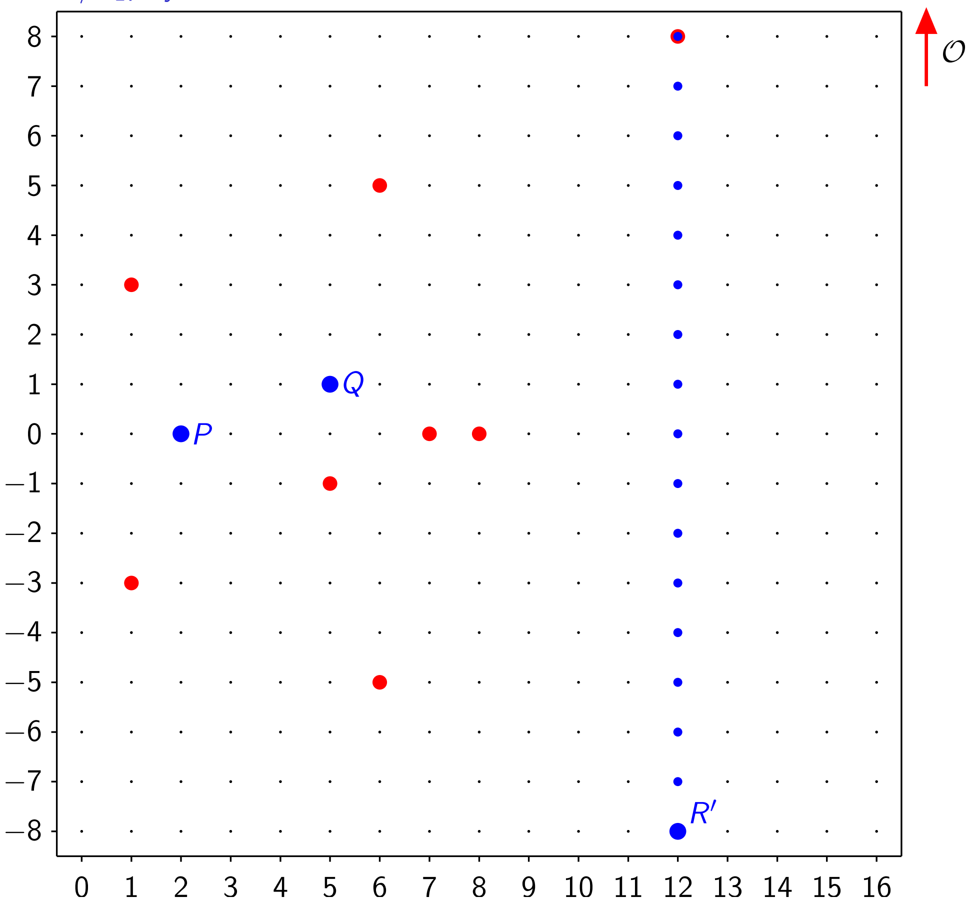

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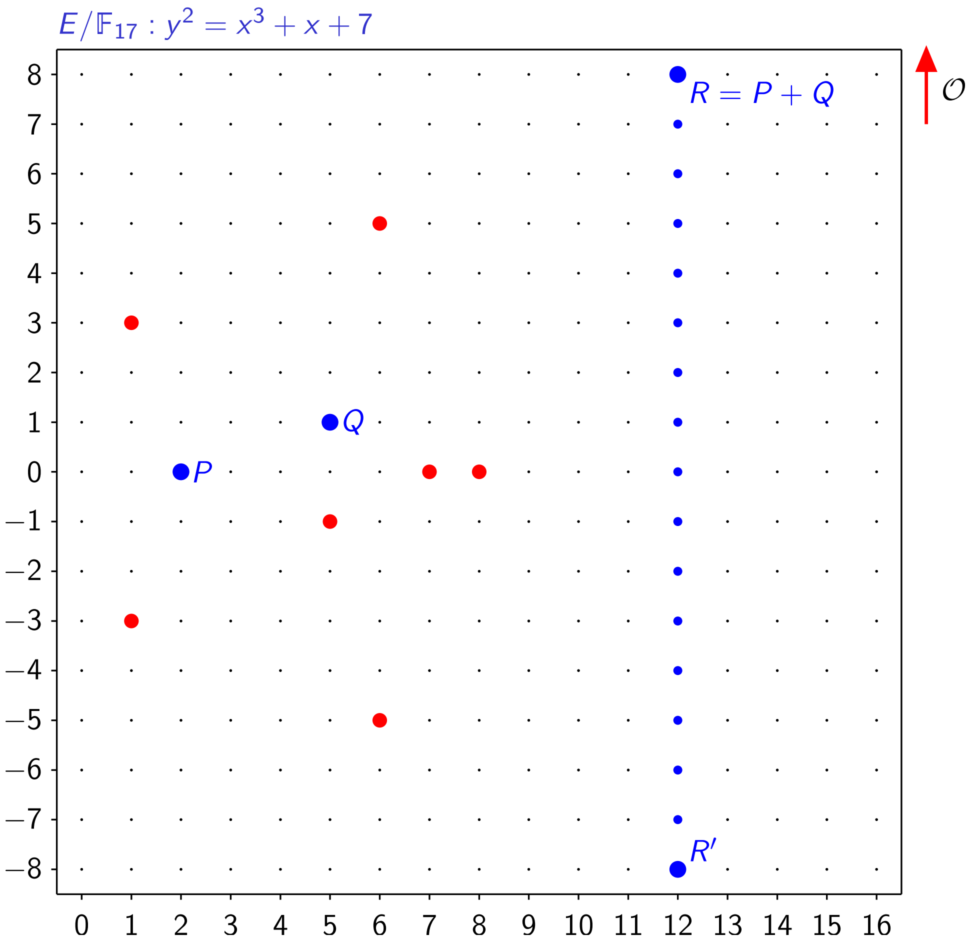

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  $\rightarrow$ Compute $\gcd(\xi, N)$ and collect a non-trivial factor!

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  - ... but also the more expensive the computation

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- Manycore processors are potentially good target architectures for ECM

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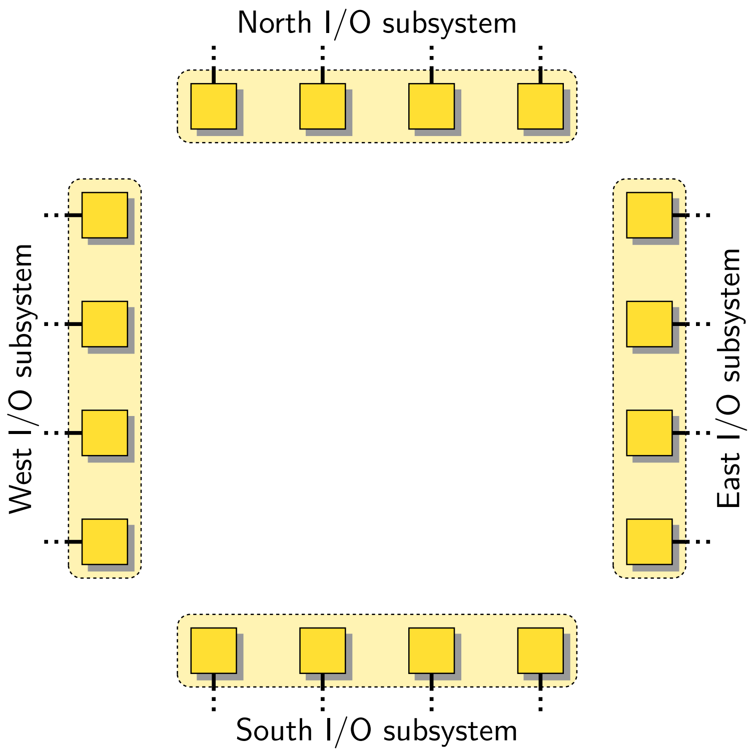

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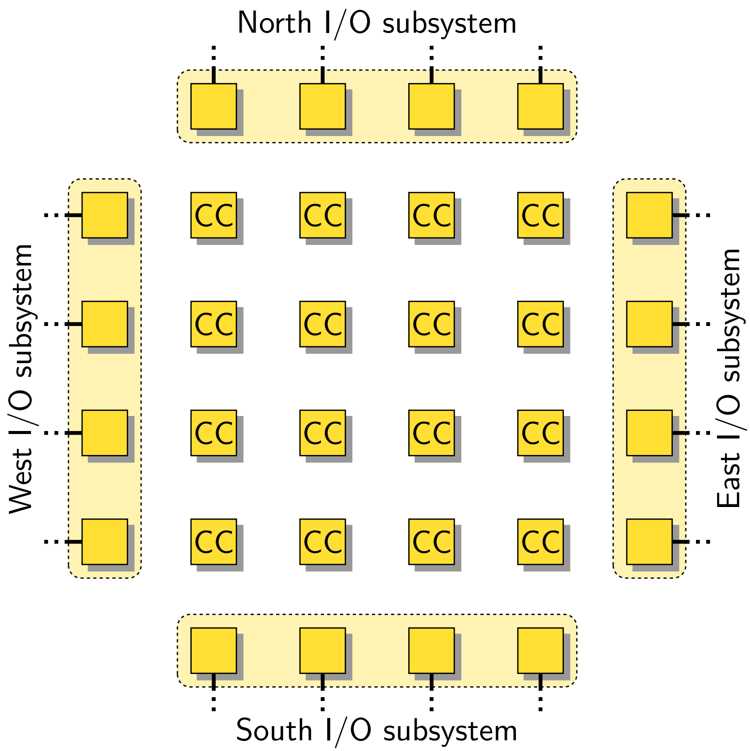

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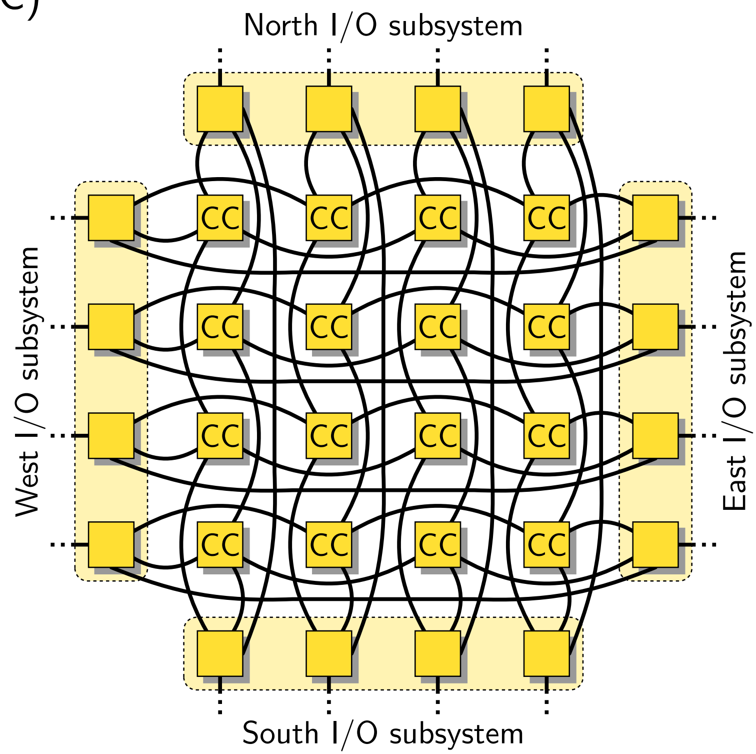
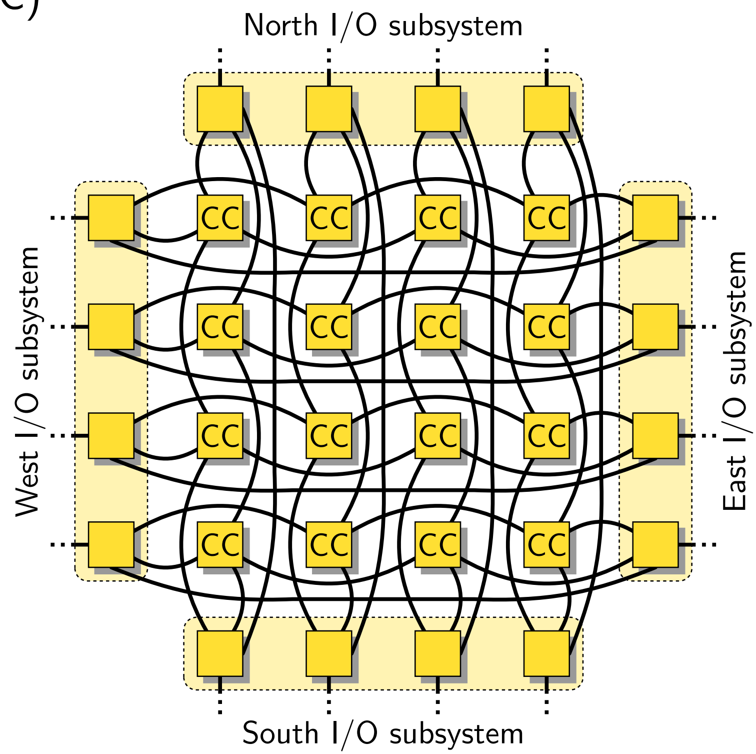


Architecture

- Global view:
  - 4 quad-core processors for I/Os (DDR RAM, PCI-e, etc.)
  - 4×4 compute clusters (CC)
  - toric network-on-chip (NoC)
  - frequency: 400 MHz
  - low power: $\leq$12-16 W



Compute clusters

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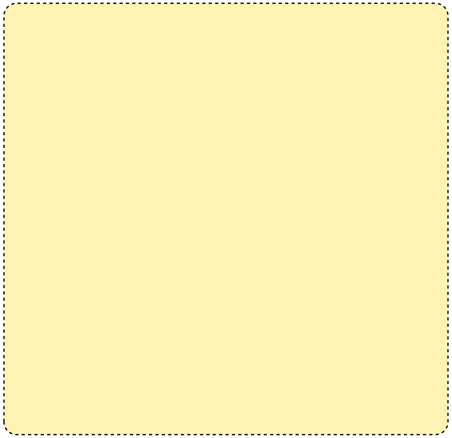

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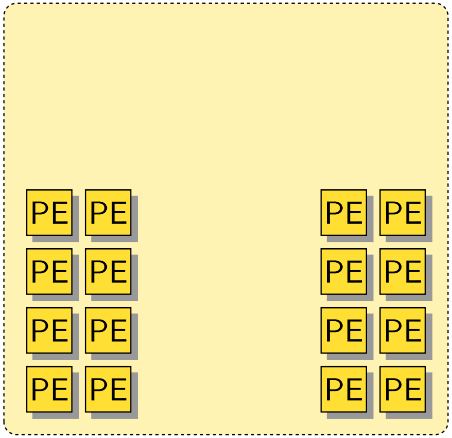
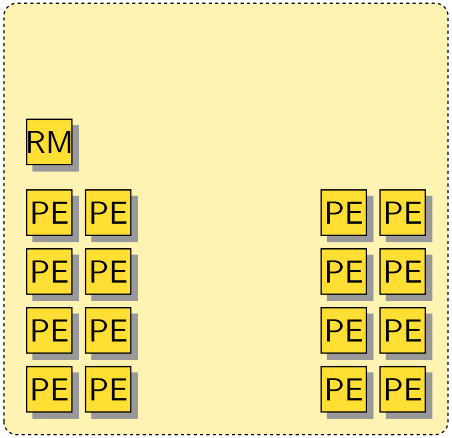


Compute clusters

- In each compute cluster:
  - 16 compute cores (PE)
  - $+$ 1 system core (RM)



Compute clusters

- In each compute cluster:
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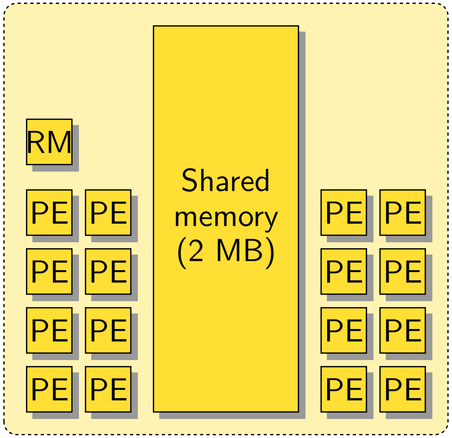

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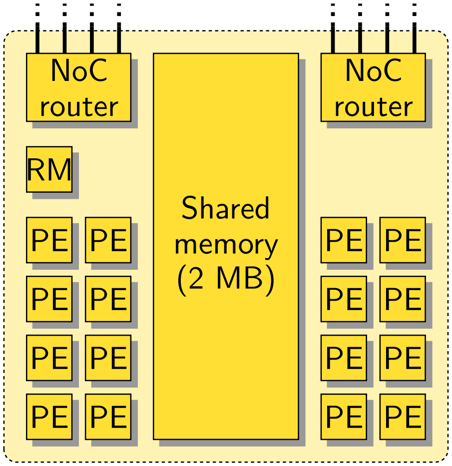

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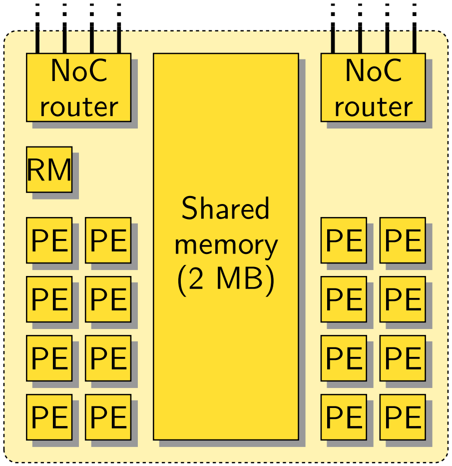
  - NodeOS (POSIX-like) + pthreads



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  - LSU (load & store) / ALU_{tiny}
  - BCU (branch & control)

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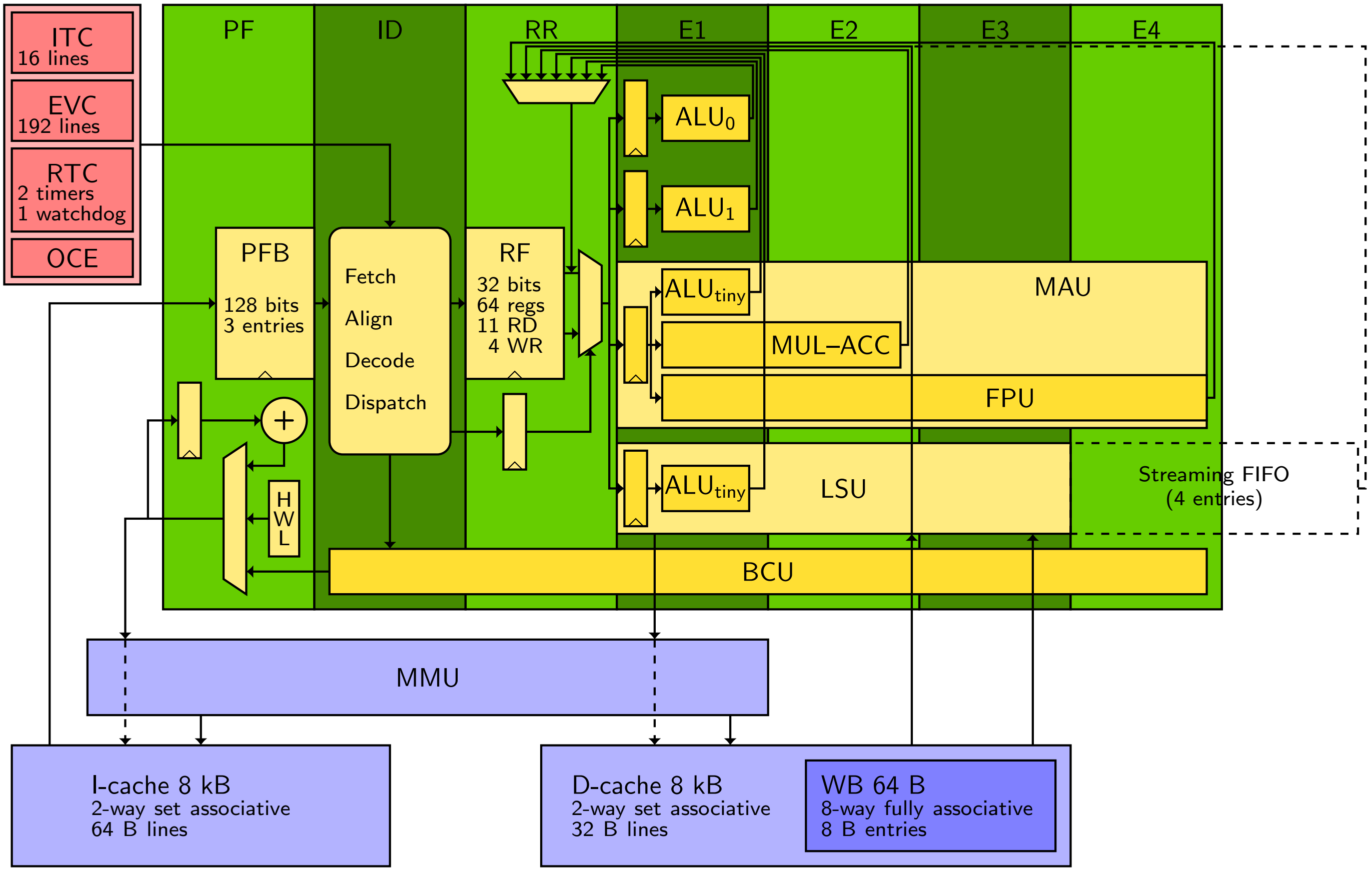

Compute core microarchitecture

- VLIW : Very Long Instruction Word
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- Low-latency instructions, along with write-back bypass:
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  - I-cache and D-cache of 8 kB each
  - fast: 32- or 64-bit cached load in 2 cycles
- Lots of useful less conventional instructions:
  - zero-penalty hardware loops
  - multiplication of 8×8 matrices over $\mathbb{F}_2$
  - arbitrary boolean functions $\{0,1\}^4 \to \{0,1\}^2$, vectorized on 32 bits
  - etc.

Development

- Toolchain: `k1-gcc`, `k1-ld`, etc.
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- A bit of Makefile magic can take care of everything

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  - simulator + GDB
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- Optimizing critical code:
  - extensive use of assembly language
  - execution times are very stable: reproducible benchmarks
  - can predict execution times with 1-cycle accuracy

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  ⇒ pack instruction bundles with `nops` to maintain code alignment
- MAU: accumulator and result have to be pairs of registers $\$\mathtt{r}_{2i}$:$\$\mathtt{r}_{2i+1}$

  ⇒ if need be, use an explicit 64-bit addition to avoid this constraint

Outline of the talk

- ECM in a nutshell
- The Kalray MPPA-256 processor
- Multiprecision modular arithmetic
- Results and conclusion

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  - additions / subtractions modulo N
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$\Rightarrow$ Write an optimized library for multiprecision modular arithmetic

- all low-level functions (add, sub, mul, etc.) in pure ASM
- higher-level functions (GCD, modular inversion) in C
- no multi-threading: all computations on a single compute core

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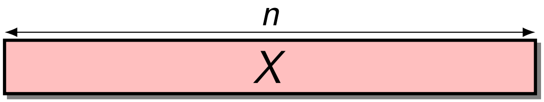

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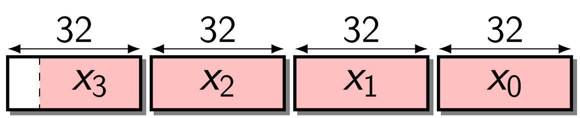
  - split X into $n_W = \lceil n/32 \rceil$ 32-bit words (or limbs):

$$X = x_{n_W-1}2^{32(n_W-1)} + \cdots + x_1 2^{32} + x_0$$



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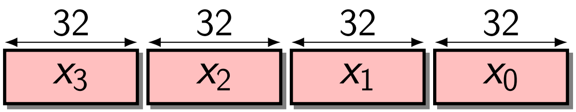

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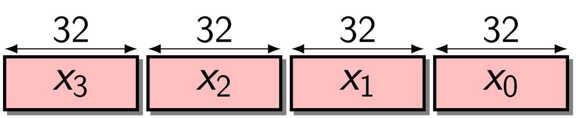
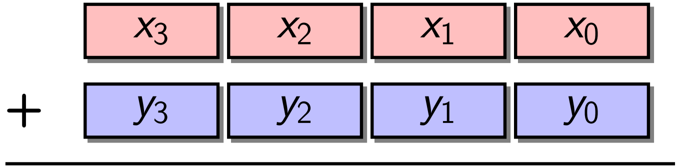
- In our library, n_W is fixed at compile-time:
  - `uint32_t` $X[n_W]$
  - supported values: $2 \leq n_W \leq 16$, i.e. from 64 to 512 bits
  - write (or generate) code optimized for each value of n_W



Multiprecision addition

- addn(R, X, Y): addition of two n_W-word integers X and Y



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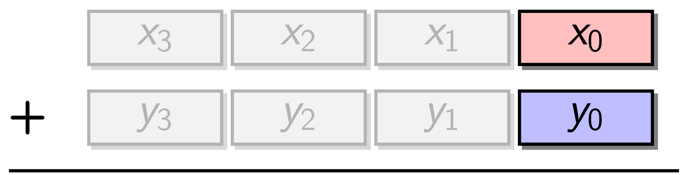

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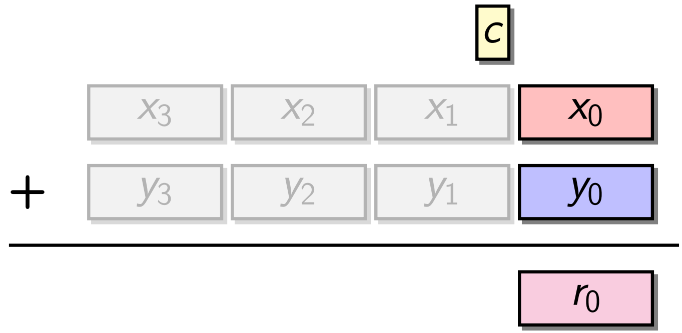

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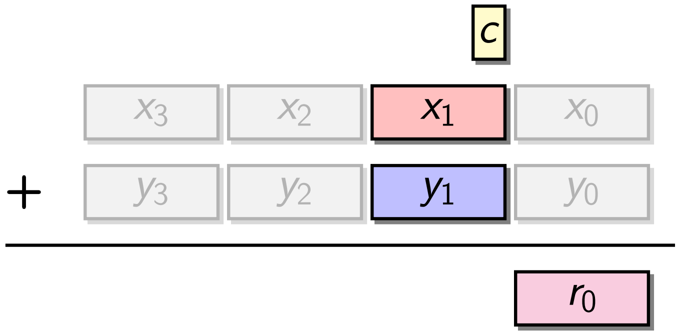

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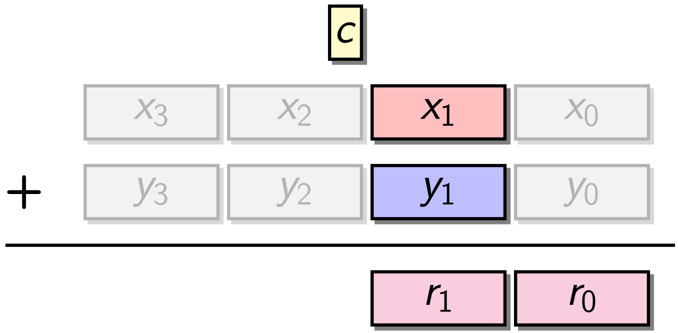

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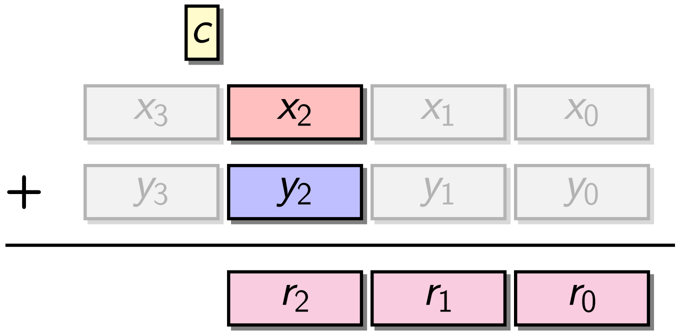

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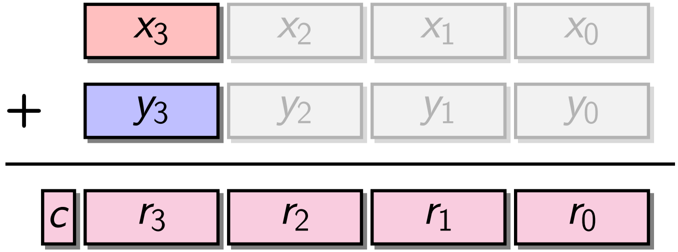

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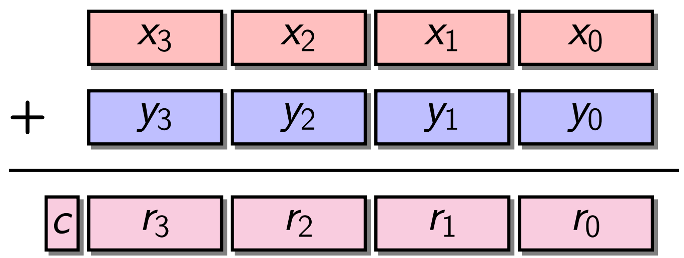

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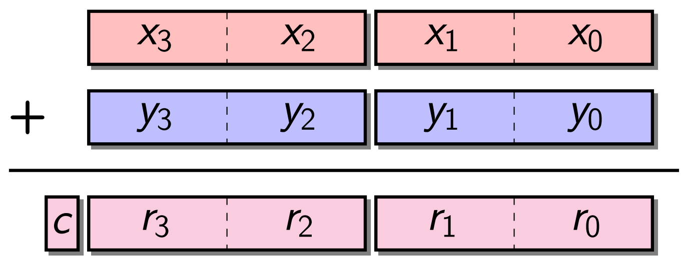

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$t+2$		$x \leftarrow$ `ld` $8(i+1)$`[`X`]`			
$t+3$		$y \leftarrow$ `ld` $8(i+1)$`[`Y`]`		$r \leftarrow$ `adddc` x`,` y	
$t+4$		$8i$`[`R`]` $\leftarrow$ `sd` r			
$t+5$				$r \leftarrow$ `adddc` x`,` y	
$t+6$		$8(i+1)$`[`R`]` $\leftarrow$ `sd` r			
$t+7$					
$t+8$					
$t+9$					
...					

Multiprecision addition

- `addn(`R`,` X`,` Y`)`: addition of two n_W-word integers X and Y
  - `ld` / `sd`: 64-bit memory accesses
  - `adddc`: 64-bit addition with carry (on ALU_0 and ALU_1)
  - total latency: $5\lceil n_W/2\rceil + O(1)$ cycles

cycle	BCU	LSU	MAU	ALU_1	ALU_0
...					
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$t+1$		$y \leftarrow$ `ld` $8i$`[`Y`]`			
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$t+3$		$x \leftarrow$ `ld` $8(i+1)$`[`X`]`		$r \leftarrow$ `adddc` x`,` y	
$t+4$		$y \leftarrow$ `ld` $8(i+1)$`[`Y`]`			
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...					
t		$x \leftarrow$ ld $8i$[X]		$r \leftarrow$ adddc x, y	
$t+1$		$y \leftarrow$ ld $8i$[Y]			
$t+2$		$8(i-1)$[R] $\leftarrow$ sd r			
$t+3$		$x \leftarrow$ ld $8(i+1)$[X]		$r \leftarrow$ adddc x, y	
$t+4$		$y \leftarrow$ ld $8(i+1)$[Y]			
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  - ld / sd: 64-bit memory accesses
  - adddc: 64-bit addition with carry (on ALU_0 and ALU_1)
  - total latency: $3\lceil n_W/2\rceil + O(1)$ cycles

cycle	BCU	LSU	MAU	ALU_1	ALU_0
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t		$x \leftarrow$ ld $8i[X]$		$r \leftarrow$ adddc x, y	
$t+1$		$y \leftarrow$ ld $8i[Y]$			
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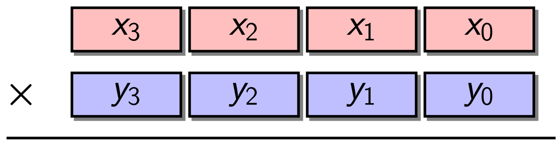
- `muln`(R, X, Y): multiplication of two n_W-word integers X and Y



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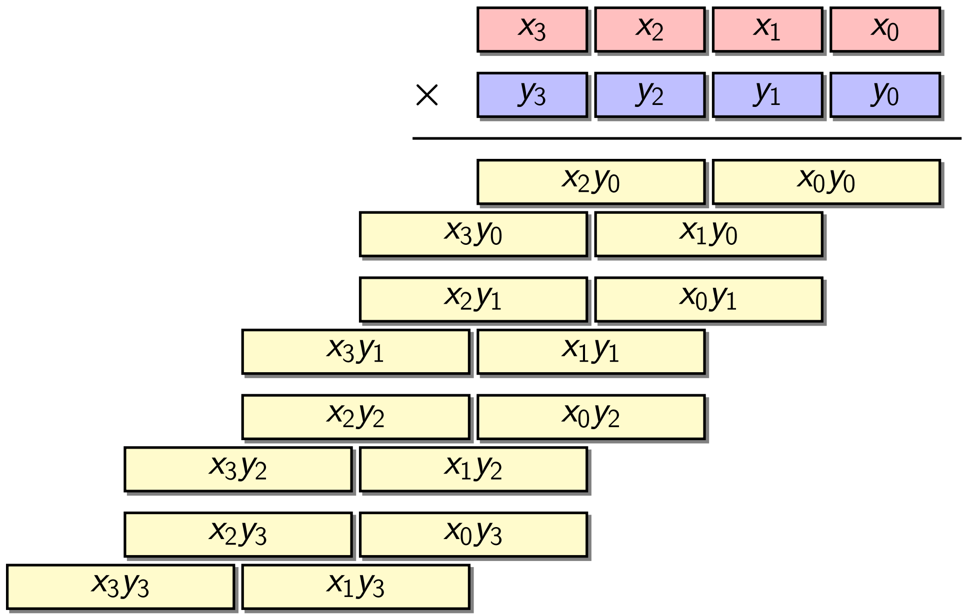

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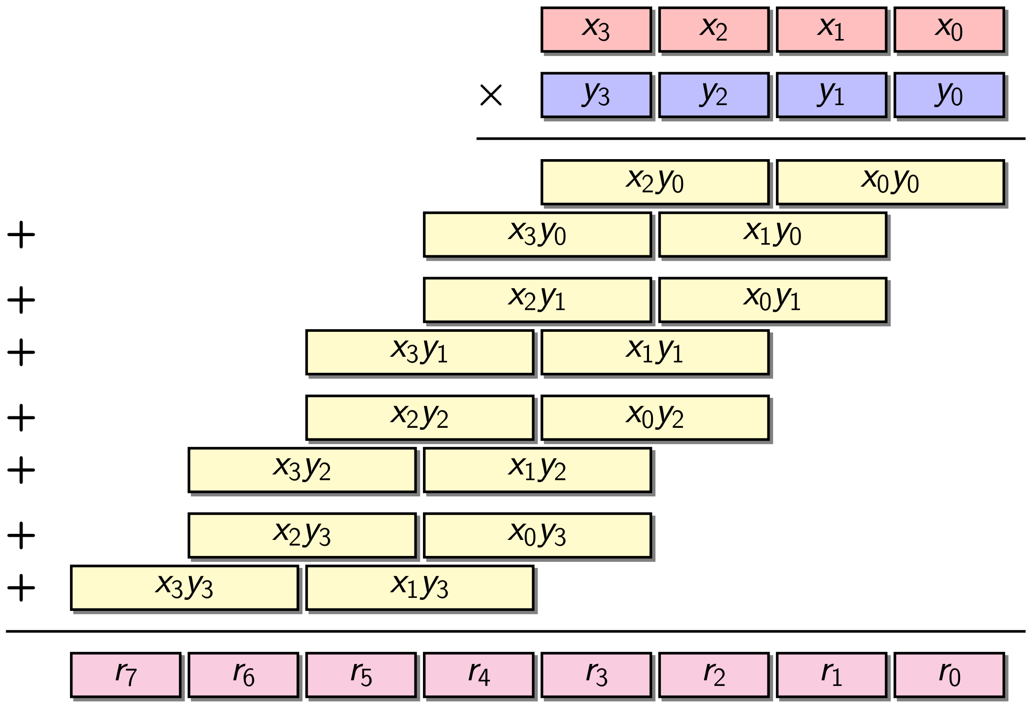

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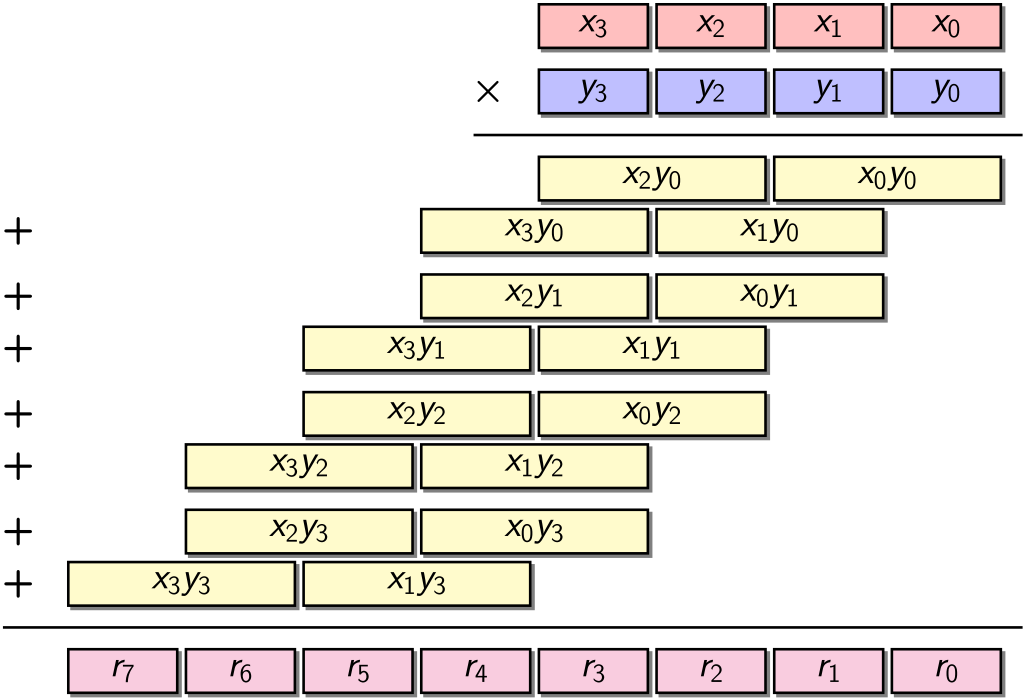

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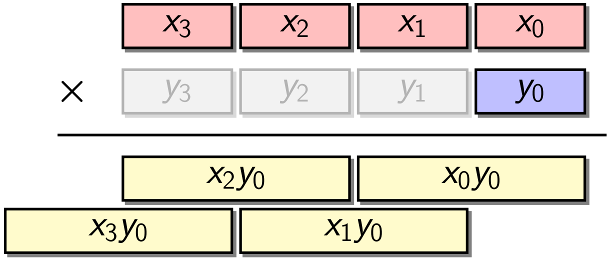

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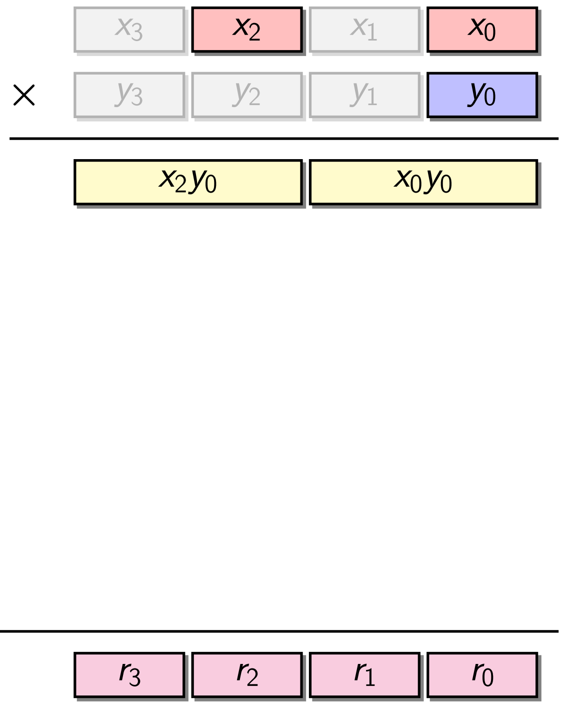

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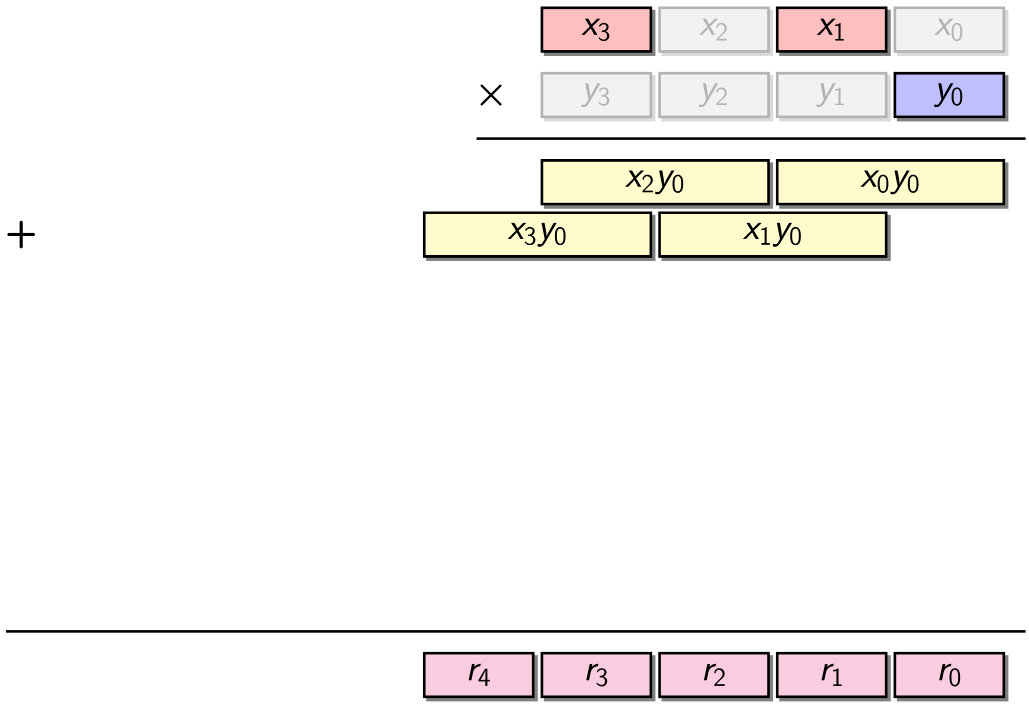

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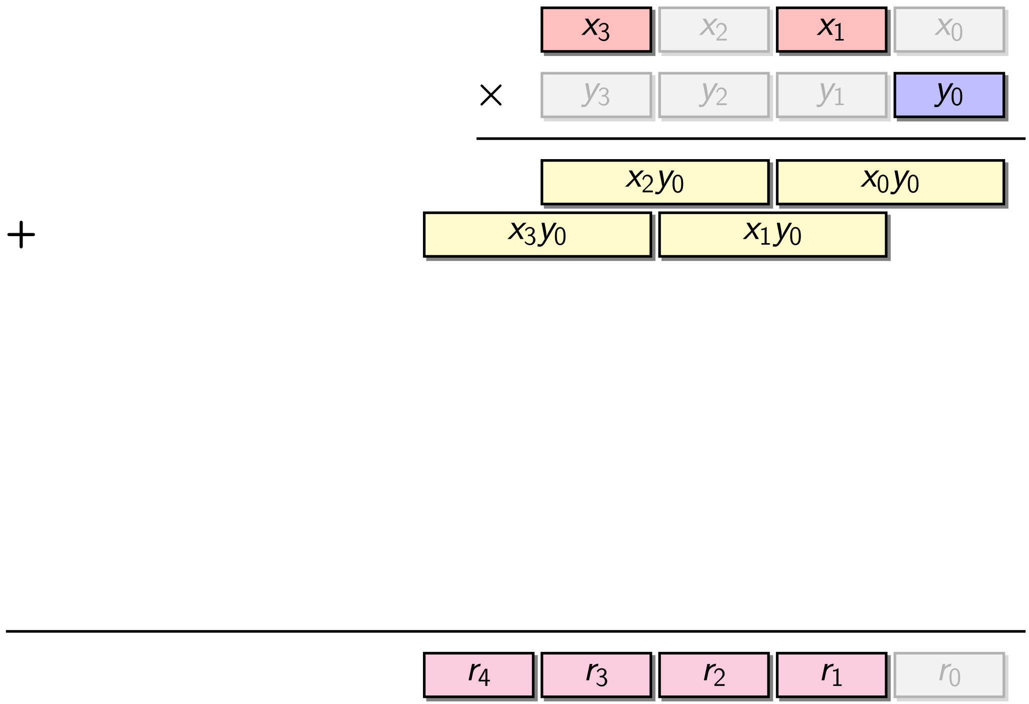

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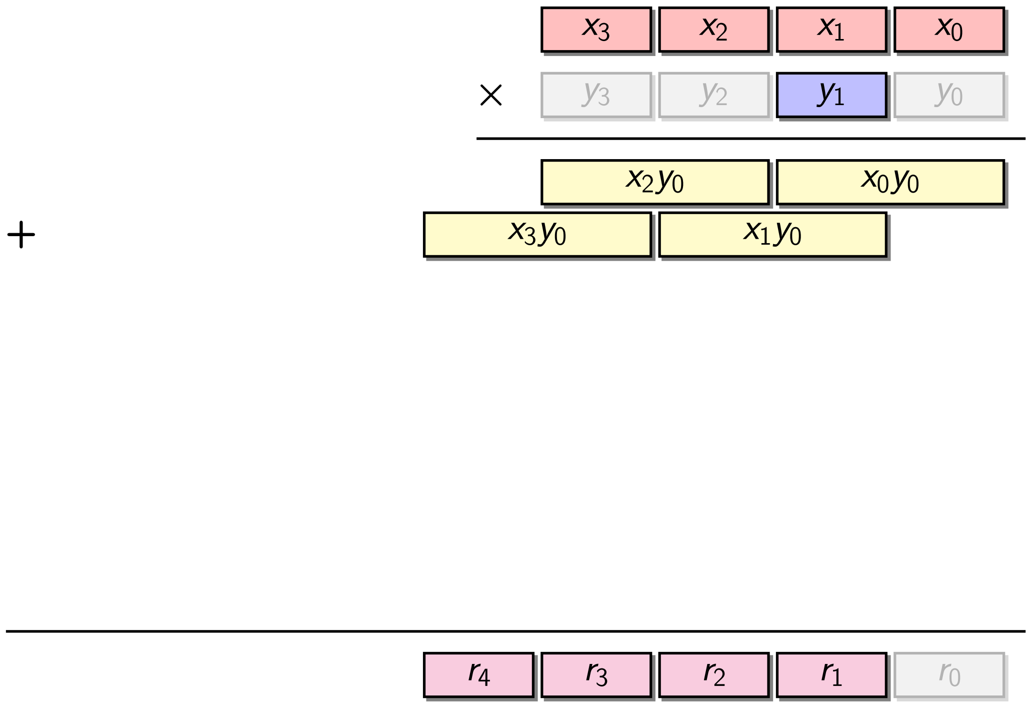

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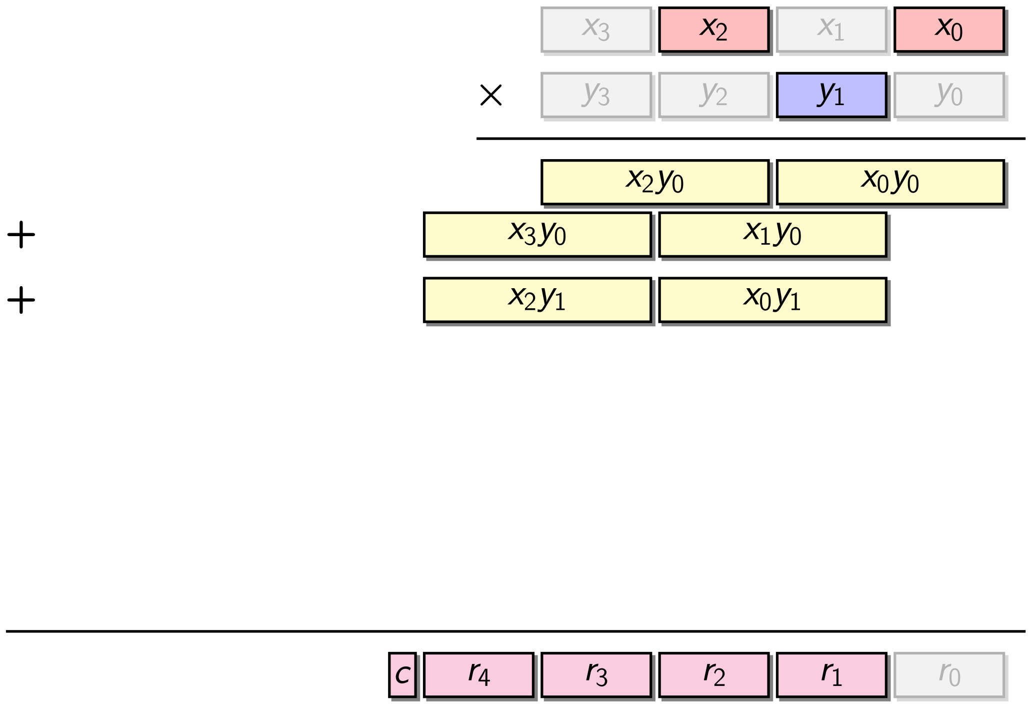

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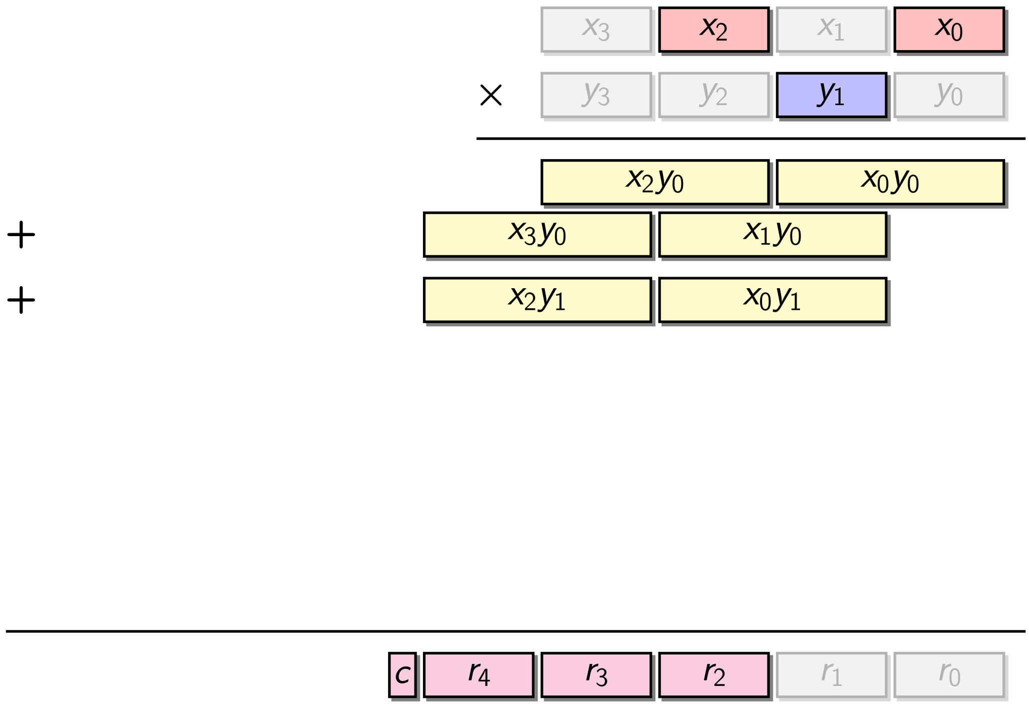

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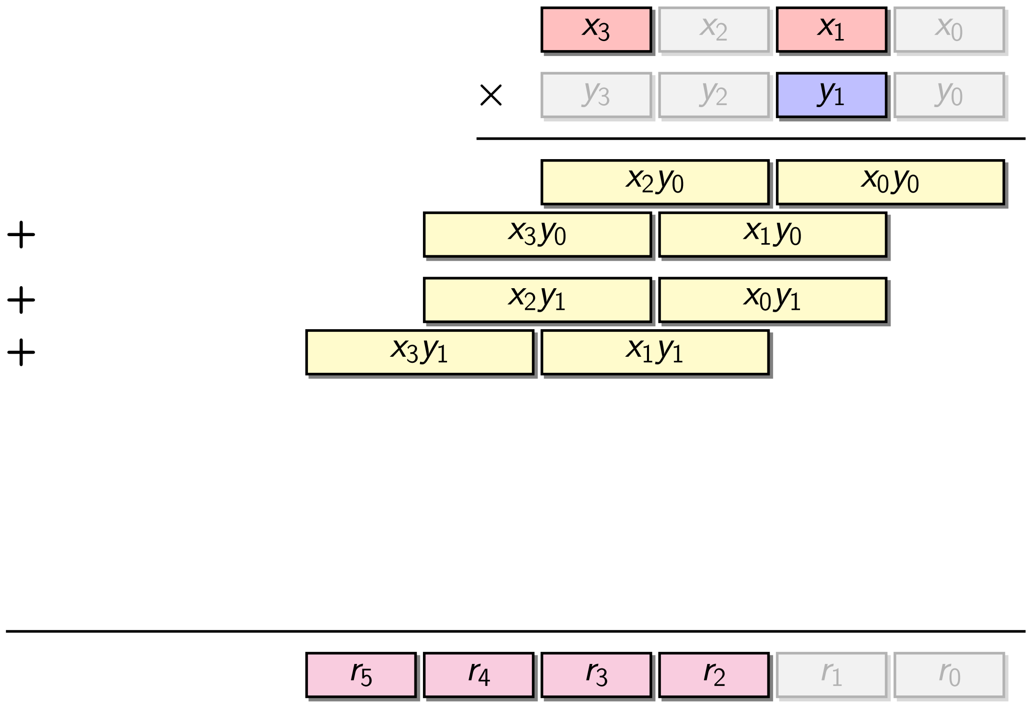

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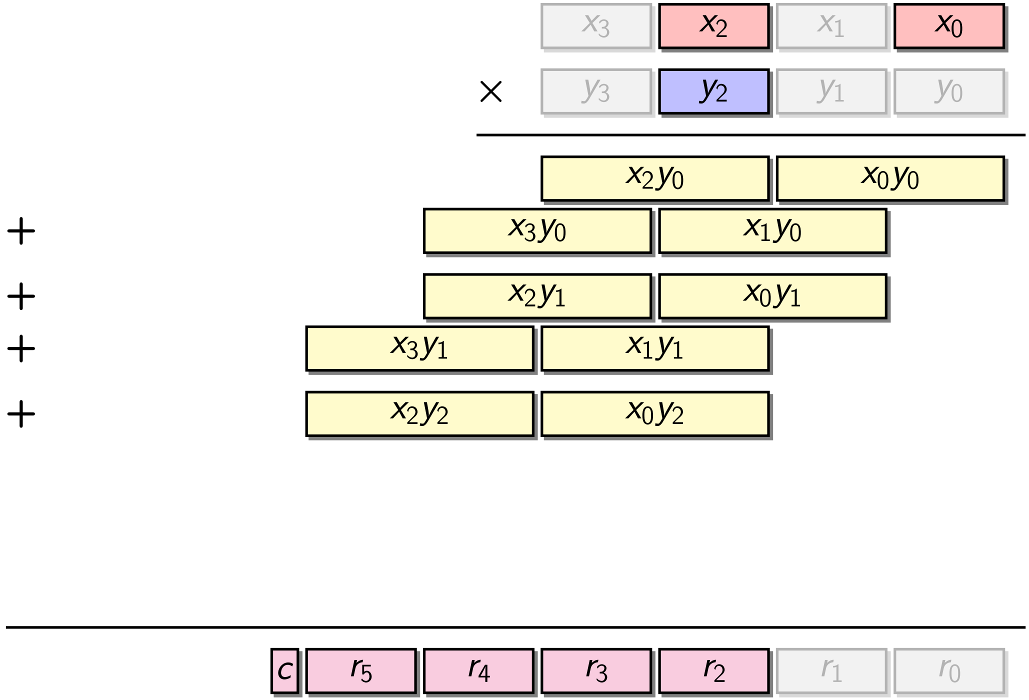

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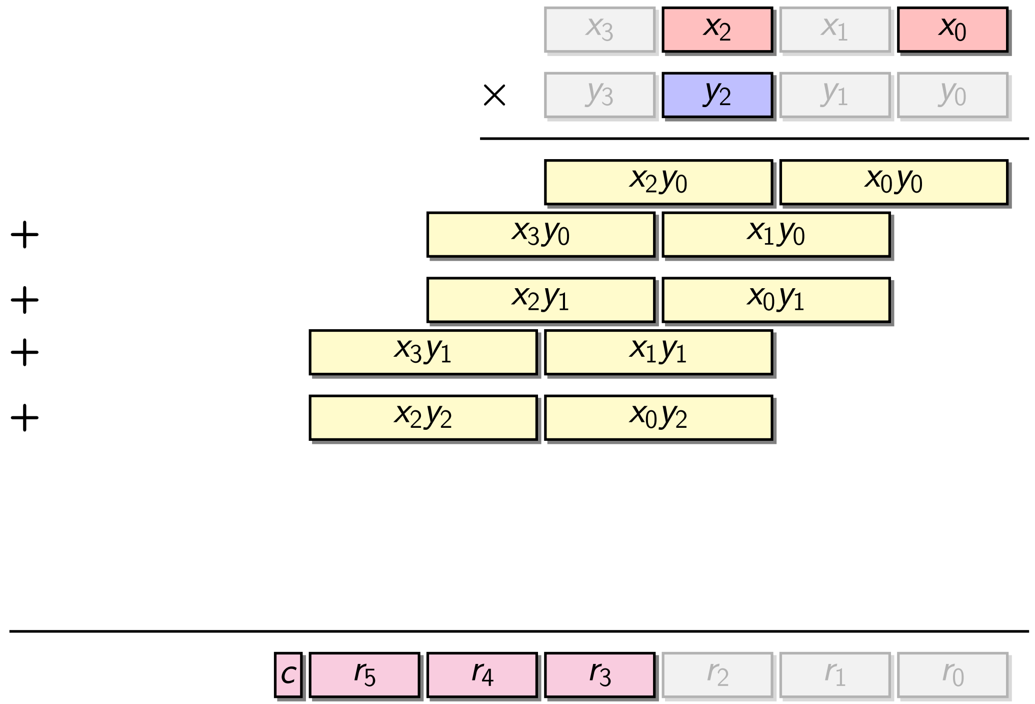

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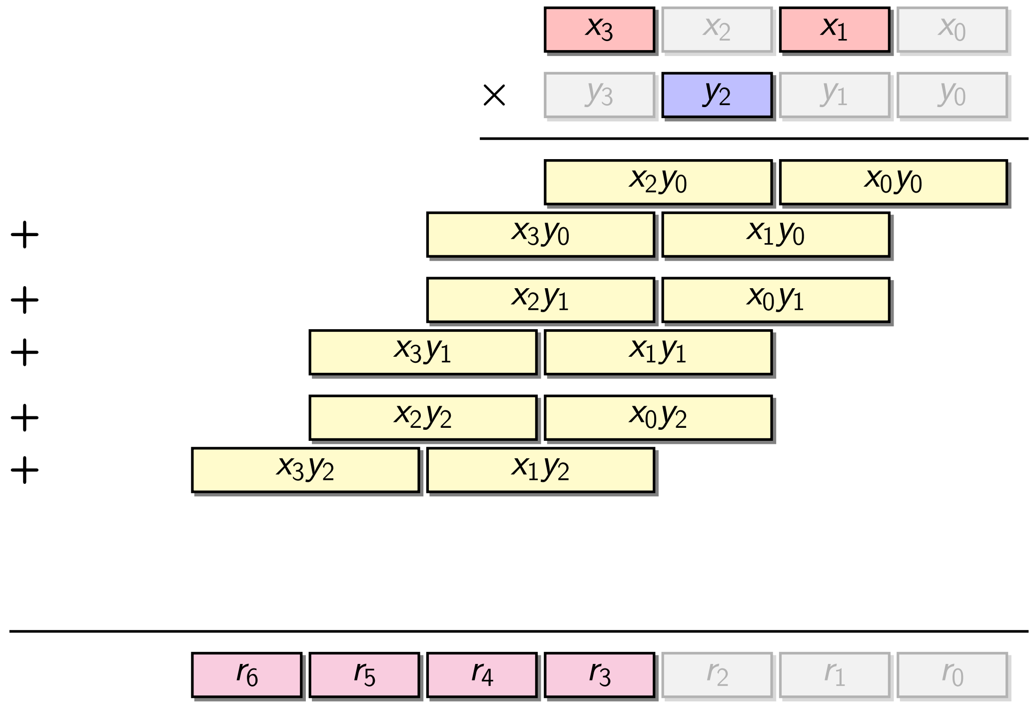

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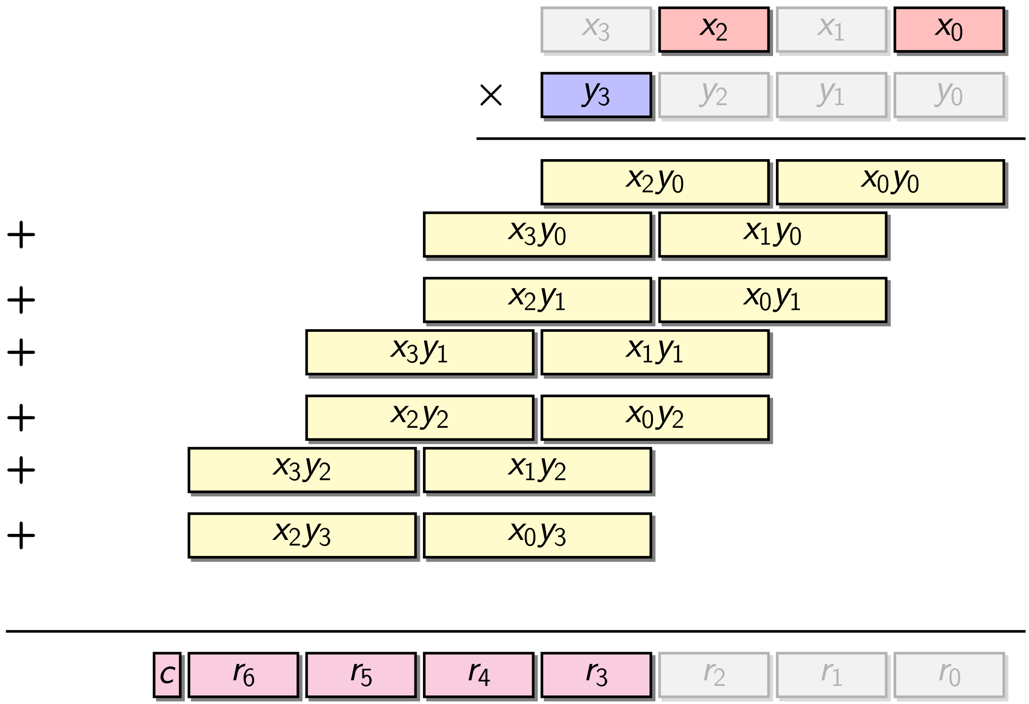

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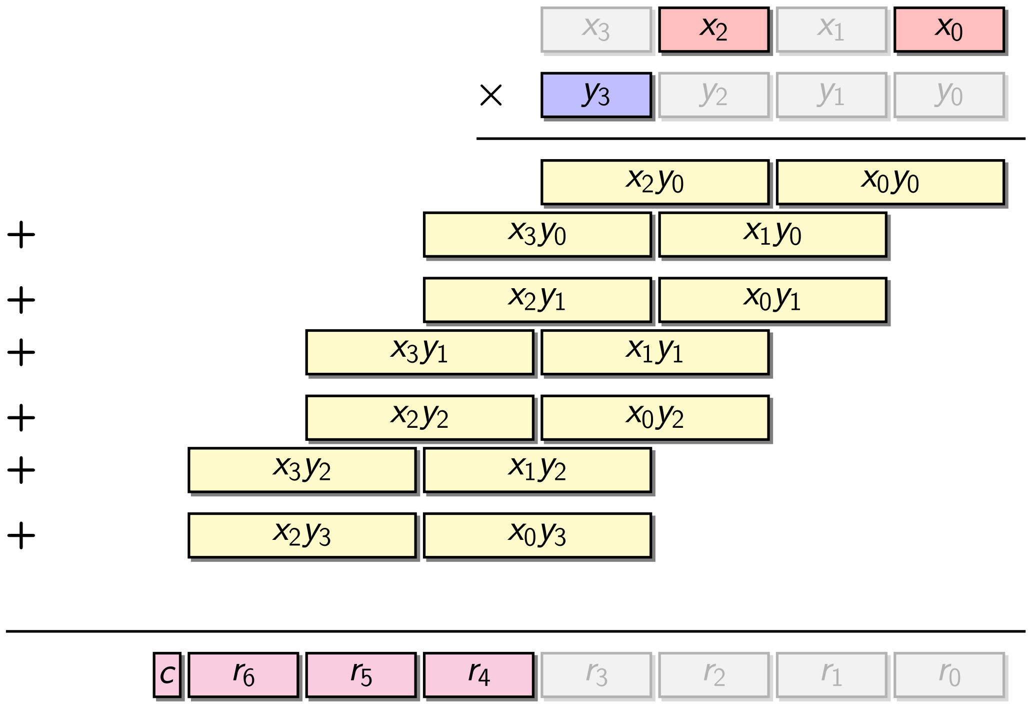

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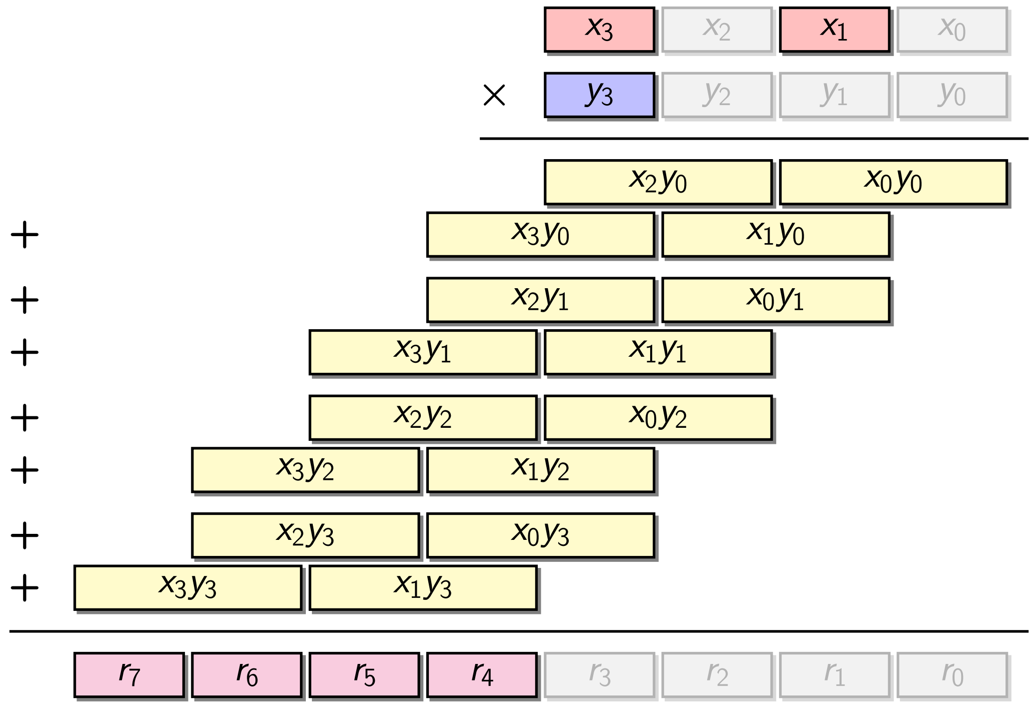

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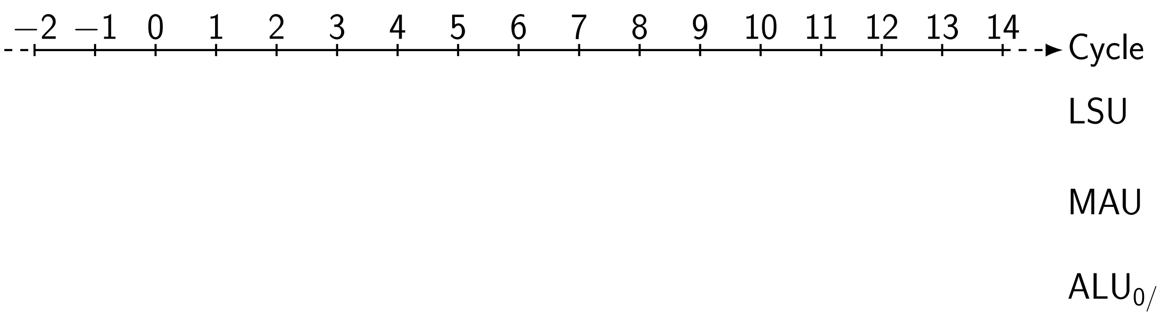

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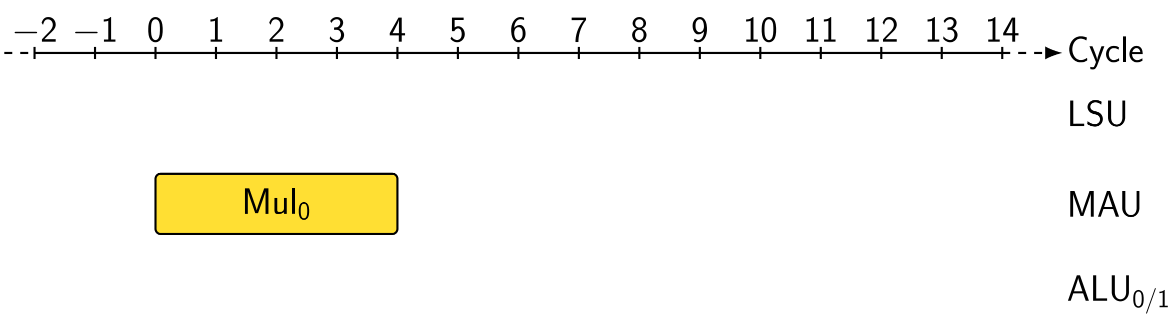

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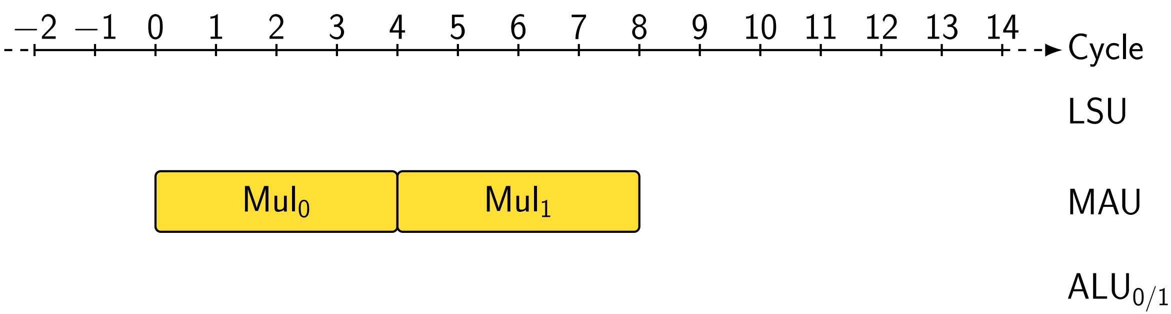

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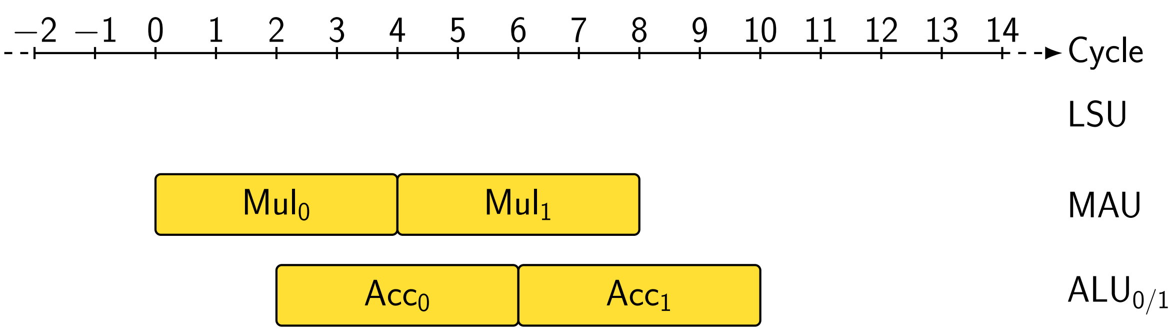

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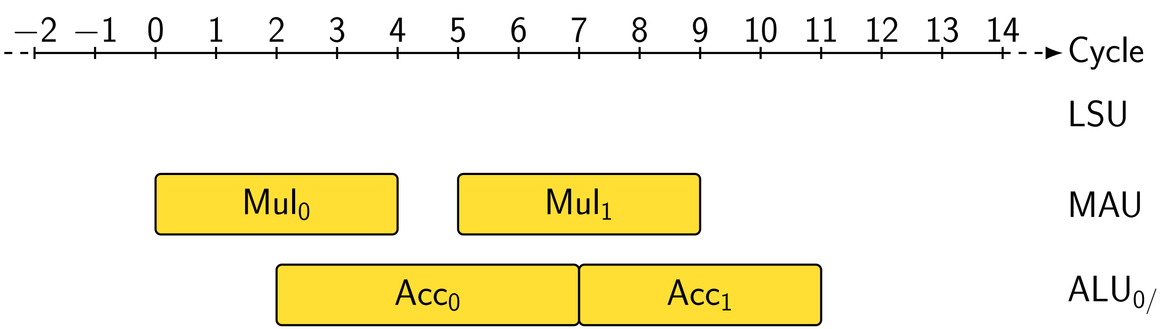

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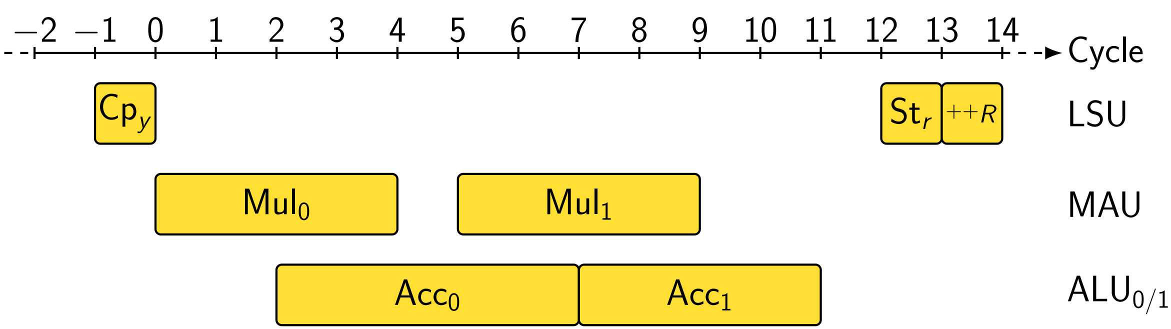

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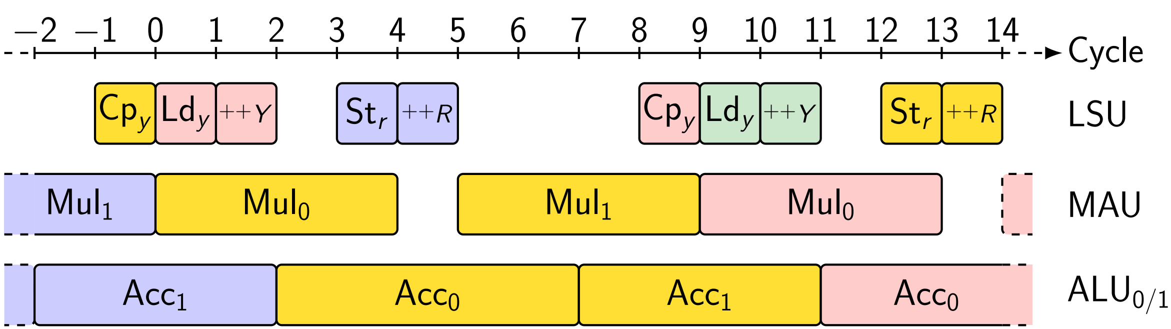

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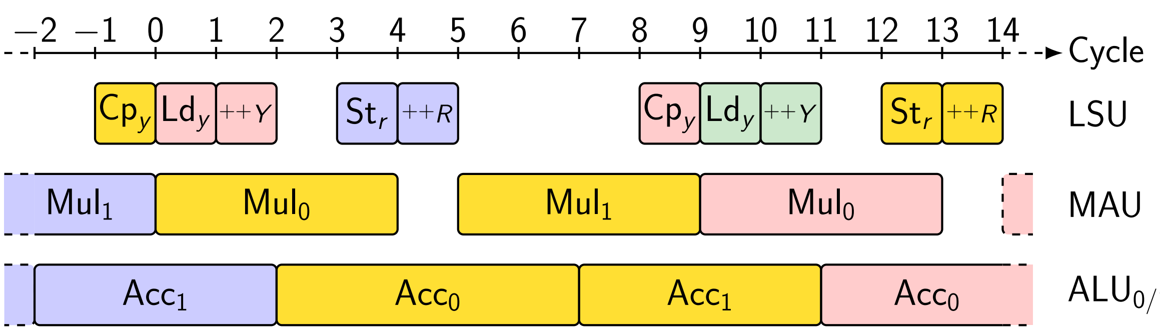
  - repeated n_W times
- Total latency: $n_W(n_W + 1) + O(1)$ cycles, **≈ 1 cycle / subproduct**



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    - $Y \leftarrow X + q \cdot N$ // `addmul_1`; $Y \equiv 0 \pmod{2^{32}}$

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  - precomputation: $\mu \leftarrow (-N)^{-1} \bmod 2^{32}$
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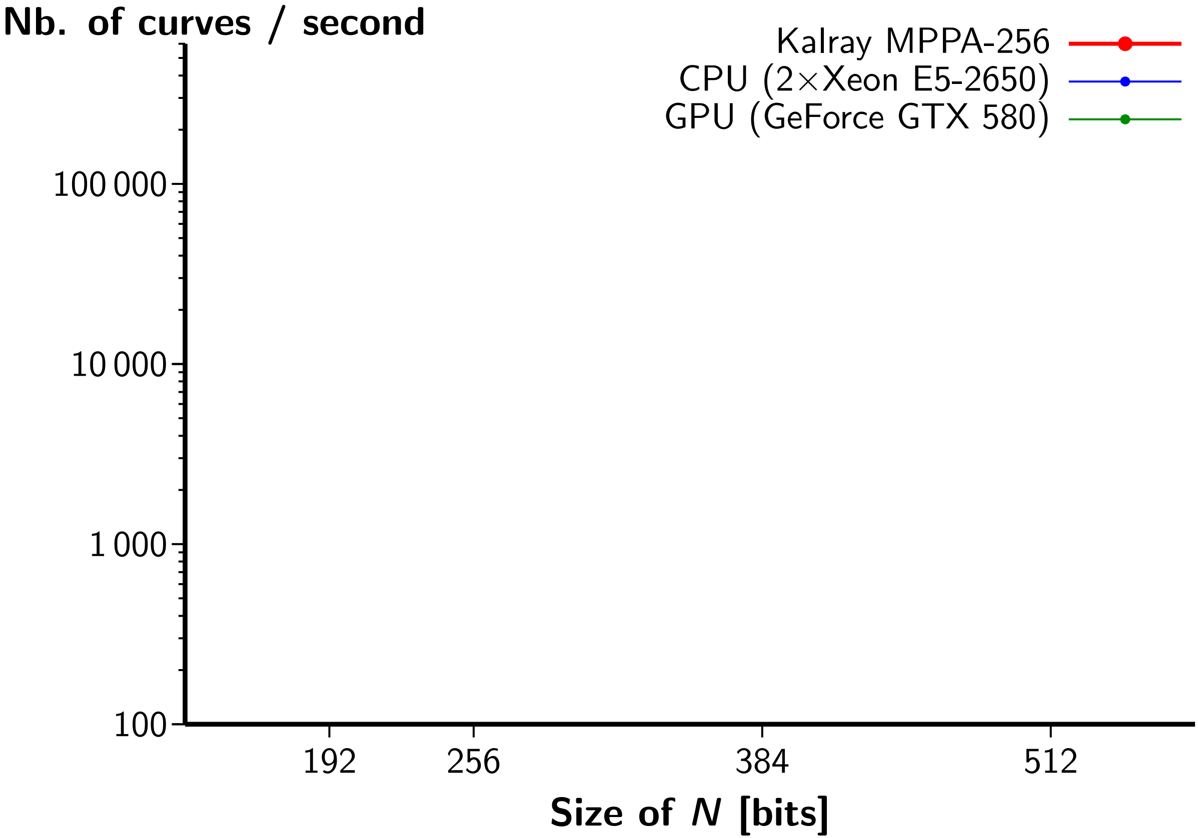
- Multiplication then REDC: $2n_W(n_W + 2) + O(1)$ cycles
  - for $n_W = 16$, in ASM: 614 cycles
  - same thing in C: 3221 cycles!

Outline of the talk

- ECM in a nutshell
- The Kalray MPPA-256 processor
- Multiprecision modular arithmetic
- Results and conclusion

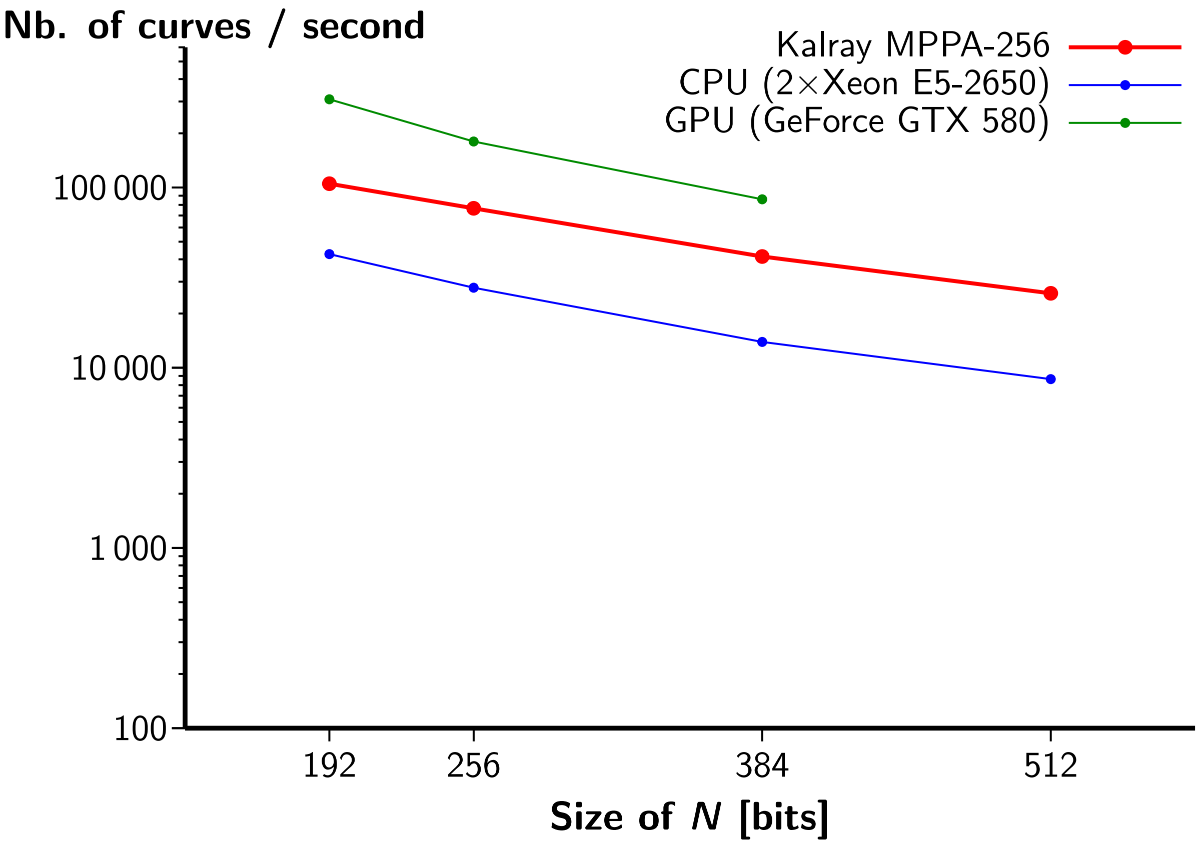
Throughput



Nb. of curves / second
Kalray MPPA-256
CPU (2×Xeon E5-2650)
GPU (GeForce GTX 580)
100 000
10 000
1 000
100
192
256
384
512
Size of N [bits]

Throughput

- ECM with $B_1 = 256$ and $B_2 = 2^{14}$ (cost: 5 381 modular mults)



Throughput

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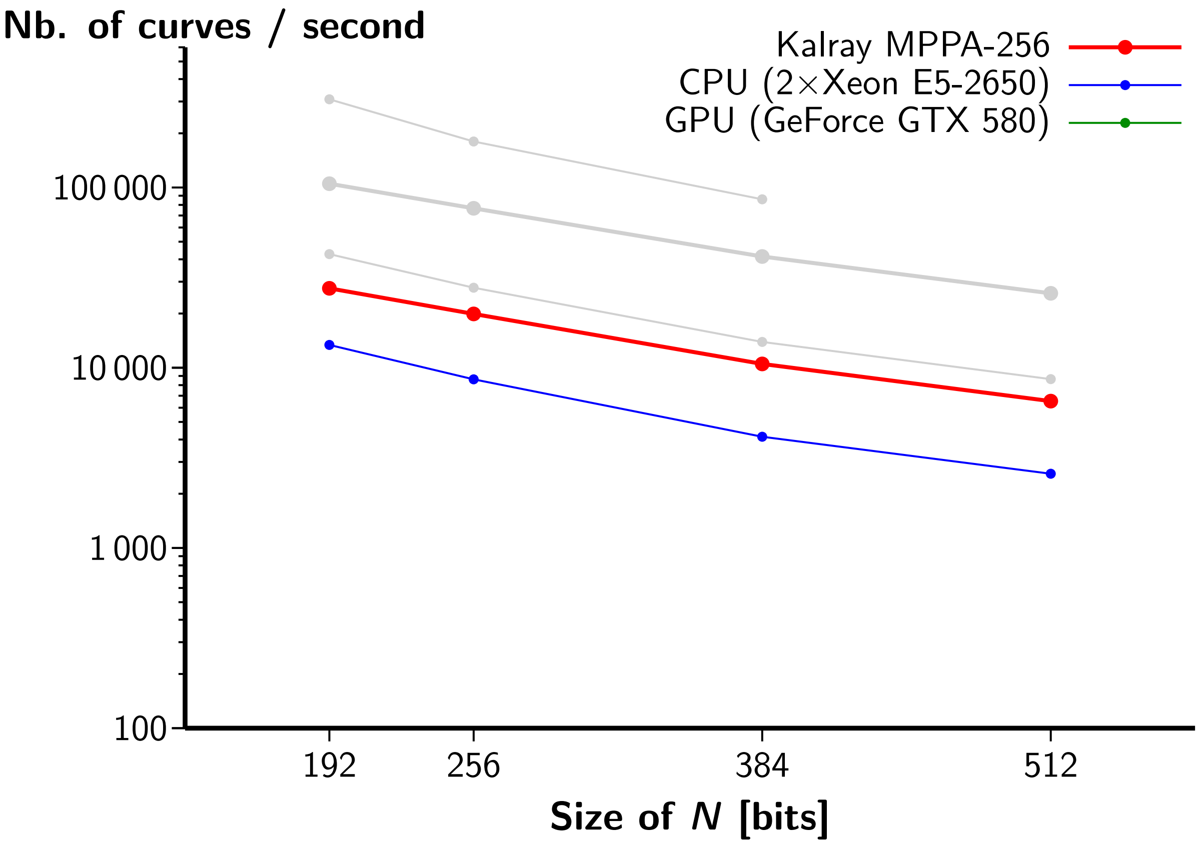

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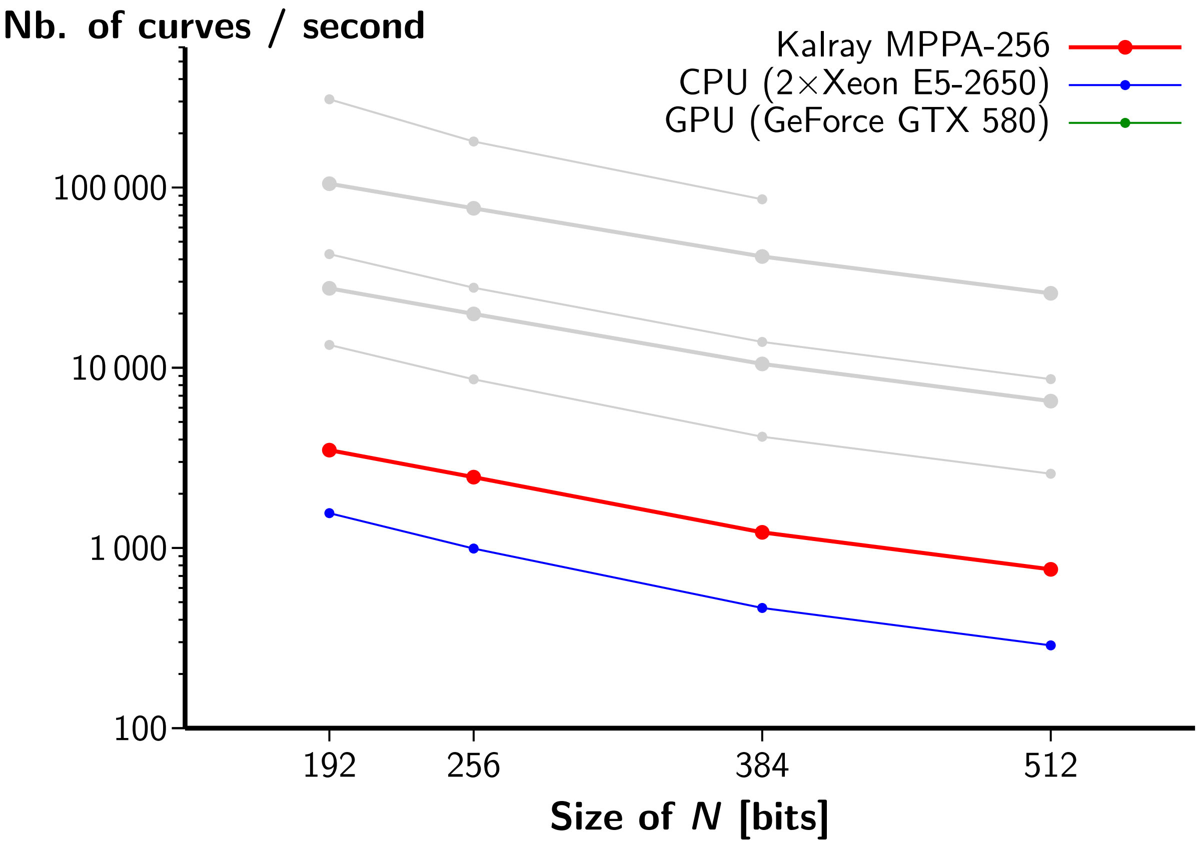

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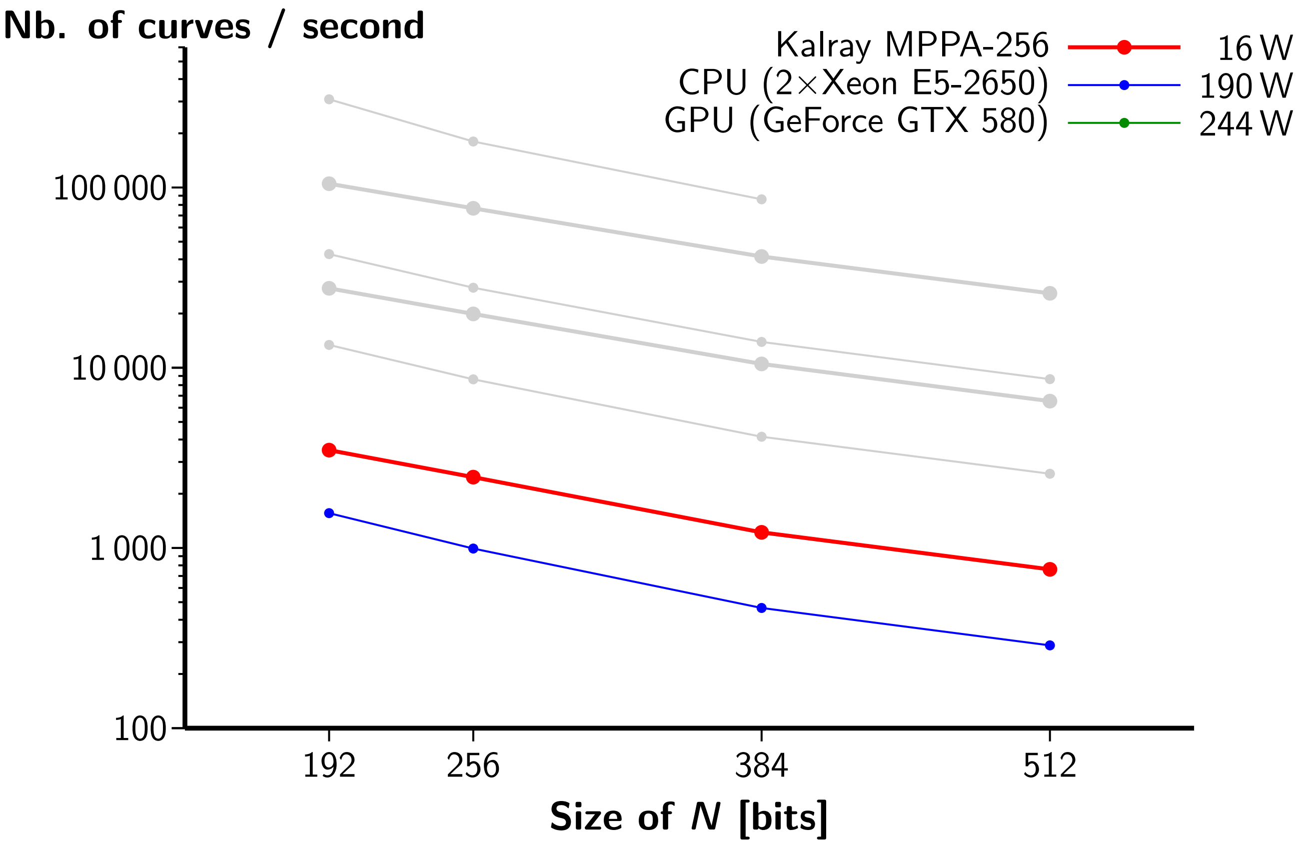
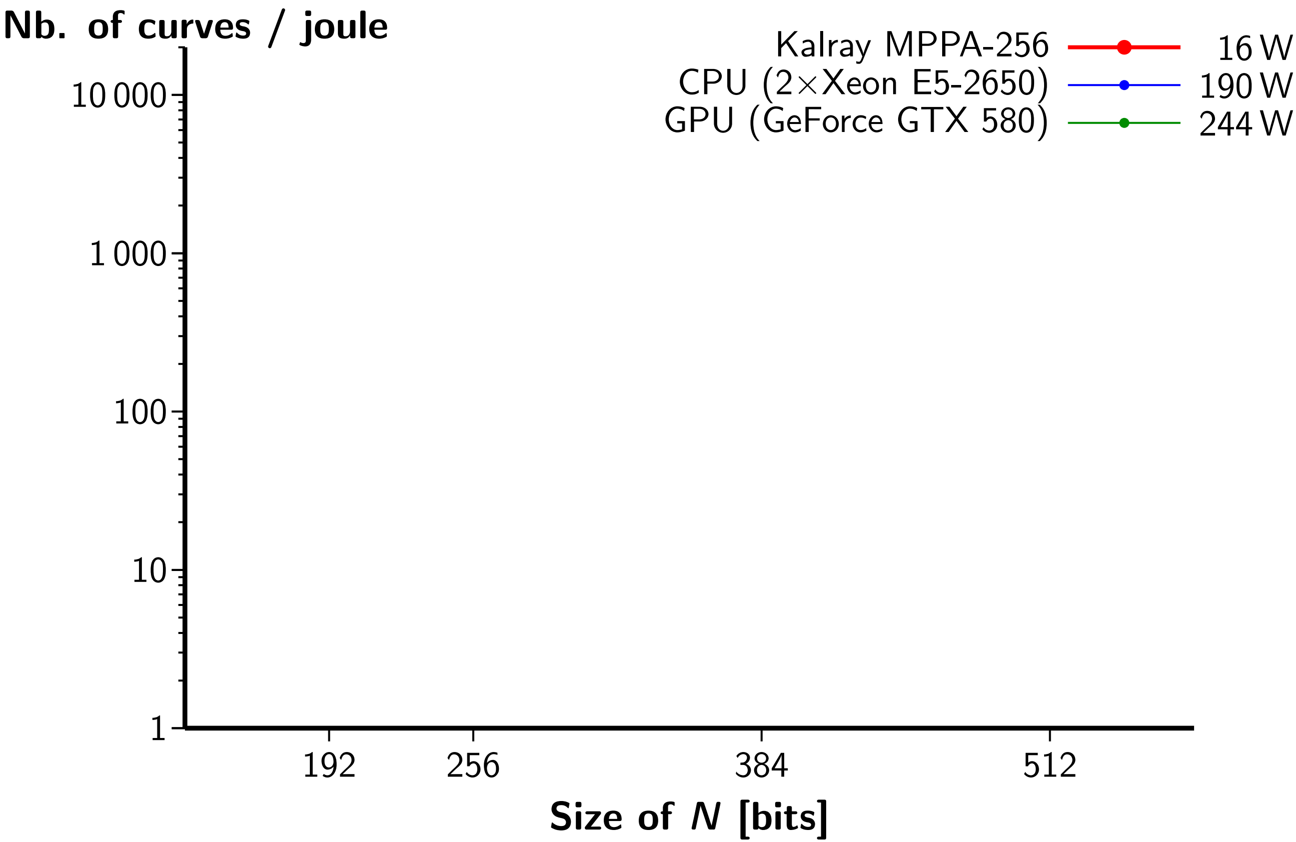


Energy efficiency



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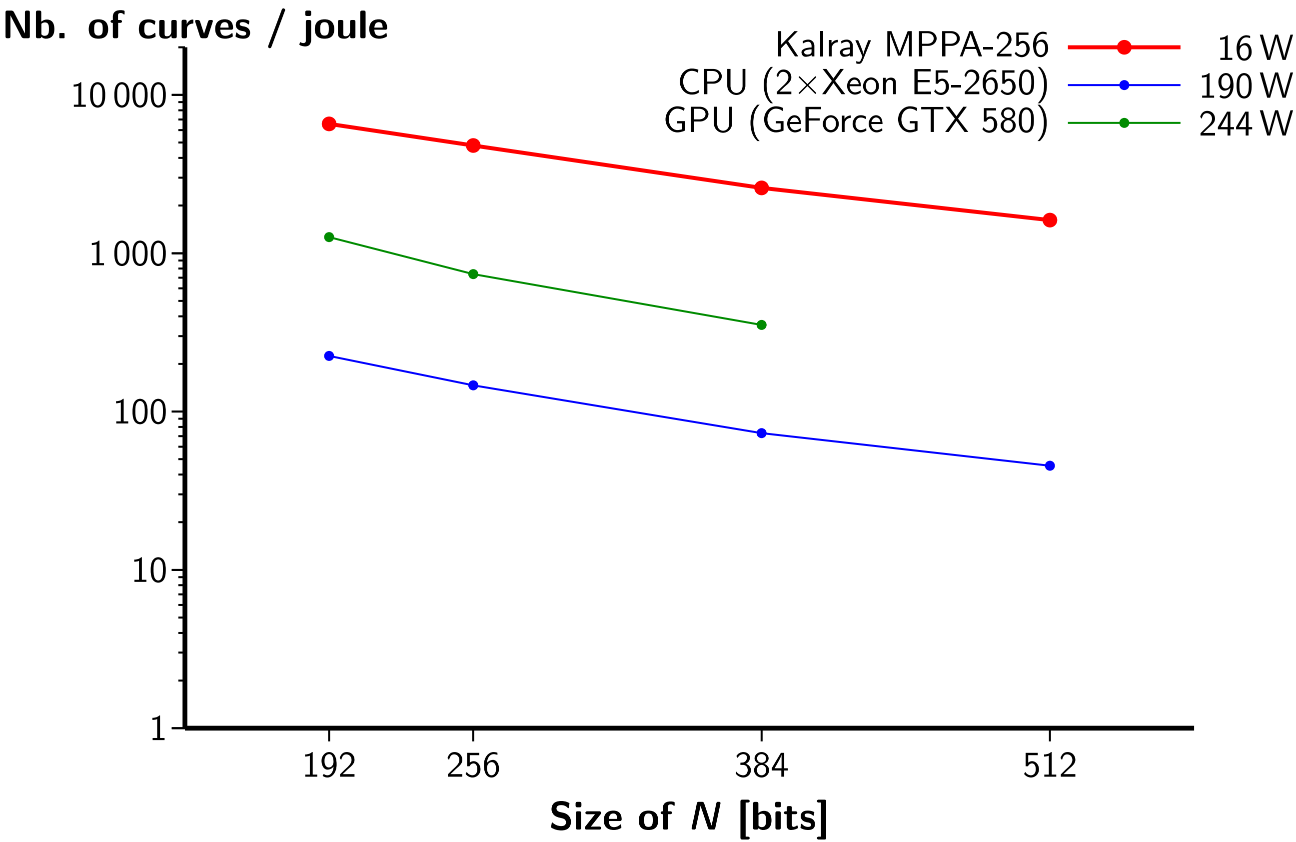

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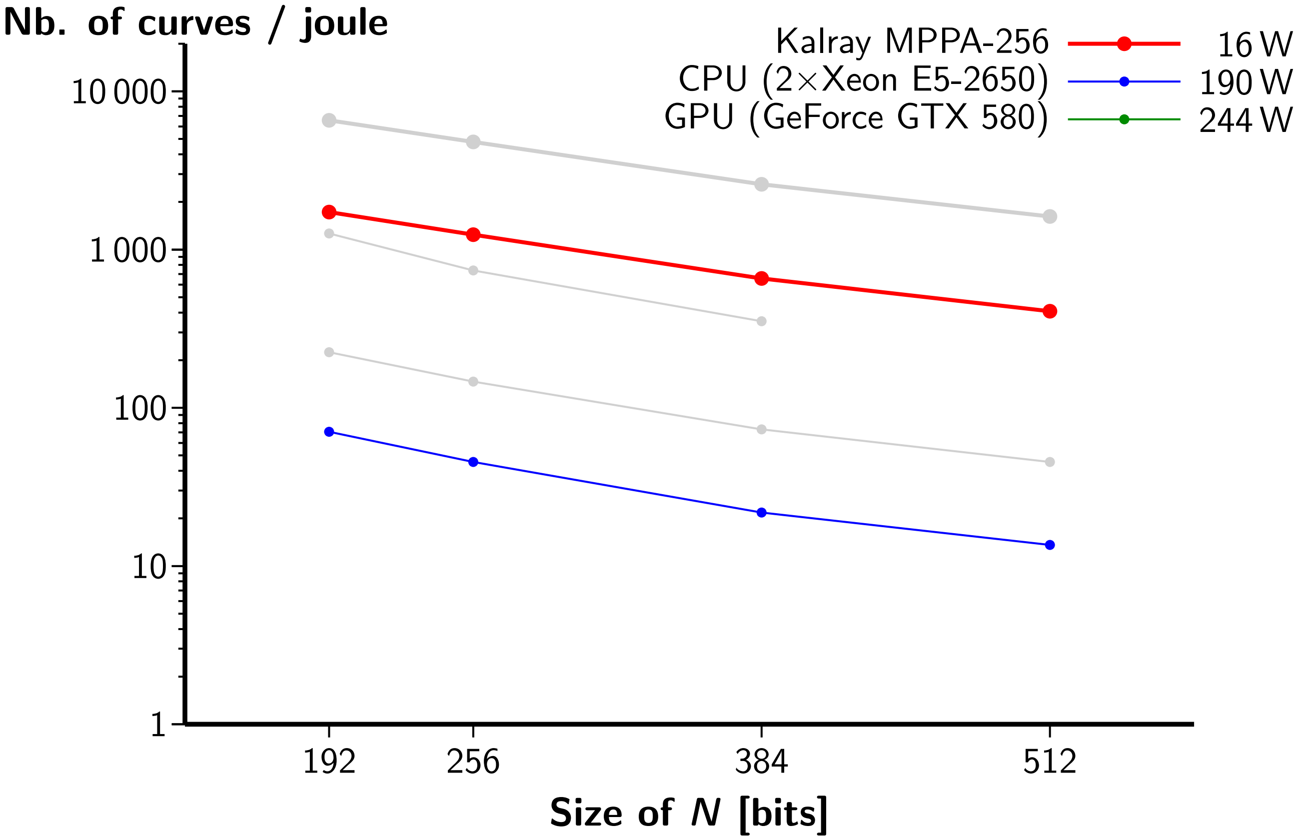

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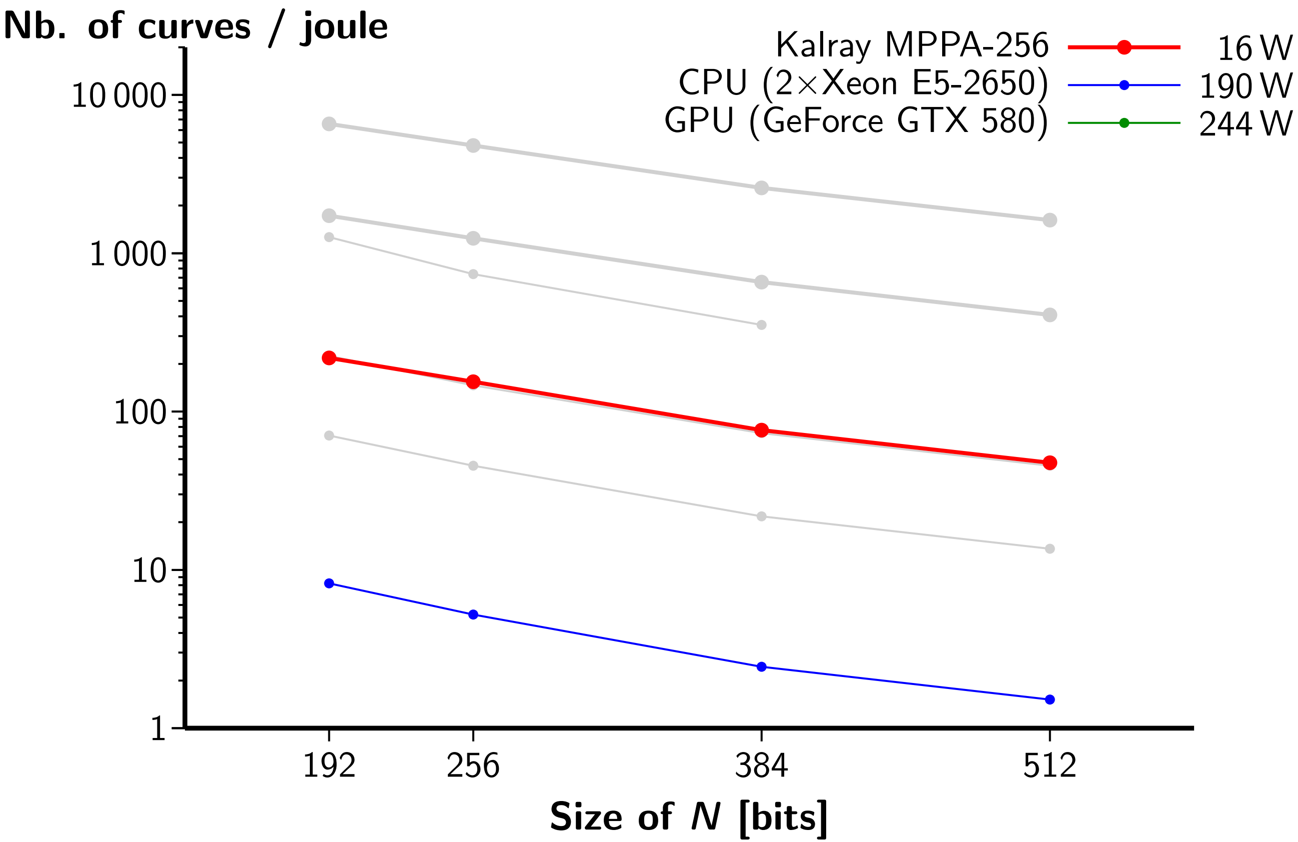

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  - energy efficient: ∼ 30× better than CPU, ∼ 5× better than GPU
  - more on-chip memory: can tackle larger sizes than GPUs

Thank you for your attention

Questions?

More info:

- Git repo: https://gforge.inria.fr/projects/kalray-ecm
- Paper: https://eprint.iacr.org/2016/365